# SiWN917 NCP Single Chip Wi-Fi® and Bluetooth® LE Wireless Secure Solutions

Silicon Labs' SiWN917 Network Connectivity Processor (NCP) is a comprehensive multi-protocol wireless sub-system. It has an integrated built-in wireless subsystem, advanced security, and integrated power-management. It has Silicon Labs' ThreadArch® 4-Threaded processor running up to 160 MHz. All the networking and wireless stacks run on independent threads of the ThreadArch®. The wireless subsystem has low-cost Complementary Metal-Oxide-Semiconductor (CMOS) integration of a multi-threaded Media Access Control (MAC) processor (ThreadArch®), baseband digital signal processing, analog front-end, calibration eFuse, 2.4GHz RF transceiver and integrated power amplifier thus providing a fully-integrated solution for a range of embedded wireless applications.

SiWN917 applications include:

- Smart Home
- Security Cameras
- HVAC
- Smart Sensors
- Smart Appliances
- Health and Fitness
- Pet Tracker

- Smart Cities
- Smart Meters
- Industrial Wearable
- Smart Buildings
- Asset Tracking
- Smart hospitals
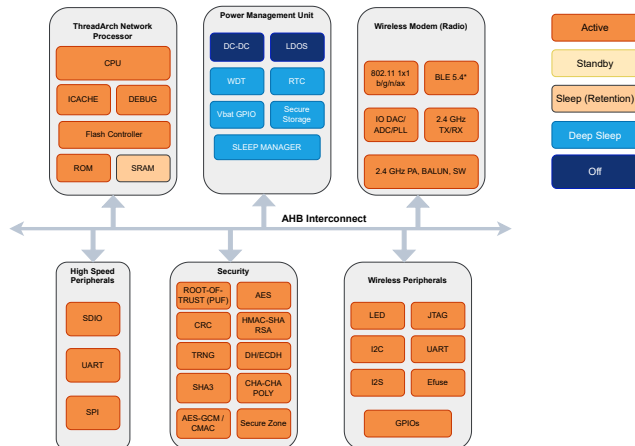
KEY FEATURES

- Wi-Fi 6 Single Band 2.4 GHz 20MHz 1x1 stream IEEE 802.11 b/g/n/ax
- Bluetooth LE 5.4
- Wi-Fi 6 Benefits: TWT for improved efficiency and longer battery life, MU-MIMO/OFDMA for Higher Throughput, network capacity and low latency
- Best in Class Device and Wireless Security
- WLAN Tx power up to +20 dBm with integrated PA
- Bluetooth LE Tx power up to +19.5 dBm with integrated PA
- WLAN Rx sensitivity as low as -97.5 dBm
- Wi-Fi Standby Associated mode current: 55 µA @ 1-second beacon listen interval
- In-package Flash up to 4MB, and support for optional external Flash
- Embedded Wi-Fi, Bluetooth LE and networking stacks supporting wireless coexistence
- Operating temperature: -40 ℃ to +85 ℃
- Wide operating supply range: 1.71 V to 3.63 V

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1. Feature List

- **Memory**
  - Embedded Static Random Access Memory (SRAM) up to 672 kB total for ThreadArch®
  - Flash up to 4 MB (in-package), up to 4 MB (External Flash).
- **Security**
  - Secure Boot
  - Secure firmware upgrade through boot-loader, Secure OTA.
  - Secure Key storage and HW device identity with PUF
  - Secure Zone
  - Secure XIP (Execution in place) from flash
  - Secure Attestation
  - Hardware Accelerators: Advanced Encryption Standard (AES) 128/256/192, Secure Hash Algorithm (SHA) 256/384/512, Hash Message Authentication Code (HMAC), Random Number Generator (RNG), Cyclic Redundancy Check (CRC), SHA3, AES-Galois Counter Mode (GCM)/ Cipher based Message Authentication Code (CMAC), Cha-Cha-poly, True Random Number Generator (TRNG)
  - Software Accelerators: RSA, ECC
  - Programmable Secure Hardware Write protect for Flash sectors
  - Anti Rollback
  - Secure Debug
- **Wi-Fi**
  - Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
  - Support for 20 MHz channel bandwidth for 802.11n and 802.11ax
  - Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi + BLE
  - Support for 802.11ax 20 MHz non-AP STA mandatory features (such as OFDMA, MU-MIMO) and optional features of individual Target wake-up time (iTWT), Broadcast TWT (bTWT)[1], Intra PPDU power save[1], SU extended range (ER), DCM (Dual Carrier Modulation). DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use , BSS Coloring, and NDP feedback upto 4 antennas
  - Transmit power up to +20 dBm with integrated PA
  - Receive sensitivity as low as -97.5 dBm
  - Data Rates: 802.11b: 1, 2, 5.5, 11; 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps ; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
  - Operating Frequency Range: 2412 MHz – 2484 MHz
  - PTA Coexistence with Zigbee/Thread/Bluetooth
- **Intelligent Power Management**
  - Power optimizations leveraging multiple power domains and partitioned sub systems
  - Many system-, component-, and circuit-level innovations and optimizations
  - Different Power Modes
  - Deep sleep mode with only timer active – with and without RAM retention

- **Bluetooth**
  - Transmit power up to +19.5 dBm with integrated PA
  - Receive sensitivity — LE: -95 dBm, LR 125 Kbps: -106 dBm
  - Operating Frequency Range — 2.402 GHz - 2.480 GHz
  - Support LE (1Mbps & 2Mbps) and LR (125Kbps & 500Kbps) rates
  - Advertising extensions
  - Data length extensions
  - LL privacy
  - LE dual role
  - BLE acceptlist
  - BLE 2 Peripheral & 2 Central connections or 1 Central & 1 Peripheral connection[1]
- **RF Features**
  - Integrated baseband processor with calibration memory
  - Integrated RF transceiver, high-power amplifier, balun and T/R switch
- **Embedded Wi-Fi Stack**
  - Support for Embedded Wi-Fi STA mode, Wi-Fi Access point mode and Concurrent (AP+STA) mode
  - Supports advanced Wi-Fi Security features: WPA Personal, WPA2 Personal, WPA3 Personal, WPA/WPA2 Enterprise in STA mode
  - Networking: Integrated IPv4/IPv6 stack, TCP, UDP, ICMP, ICMPv6, ARP, DHCP Client/Server, DHCPv6 Client, DNS Client, SSL3.0/TLS1.3 Client, SNTP, SNI
  - Applications: HTTP/s Client, HTTP/s Server[1], MQTT/s Client, AWS Client, Azure Client[1]
  - Sockets: BSD Sockets, IoT Sockets
  - Over-the-Air (OTA) Wireless firmware update
  - Provisioning using Wi-Fi AP[1] or BLE
- **Embedded Bluetooth Stack**
  - Support GAP profile
  - Support GATT profile
  - Support SMP
  - Support LE L2CAP
- **Wireless Sub-System Power Consumption**
  - Wi-Fi 4 Standby Associated mode current: 55 µA @ 1-second beacon listen interval
  - Wi-Fi 1 Mbps Listen current: 13 mA
  - Wi-Fi LP chain Rx current: 18 mA
  - Deep sleep current ~2.5 µA, Standby current (384K RAM retention) ~10 µA
- **Operating Conditions**
  - Wide operating supply range: 1.71 V to 3.63 V
  - Operating temperature: -40 ºC to +85 ºC
- **Software and Regulatory Certifications**
  - Wi-Fi Alliance: Wi-Fi 4[1], Wi-Fi 6[1]
  - Bluetooth Qualification[1]
  - Regulatory pre-certifications (FCC, IC, RED, UKCA, MIC)

Note:

1. For information about Software roadmap features and additional certification information, contact Silicon Labs for availability and timeline.
2. For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

2. Ordering Information

Table 2.1. List of OPNs

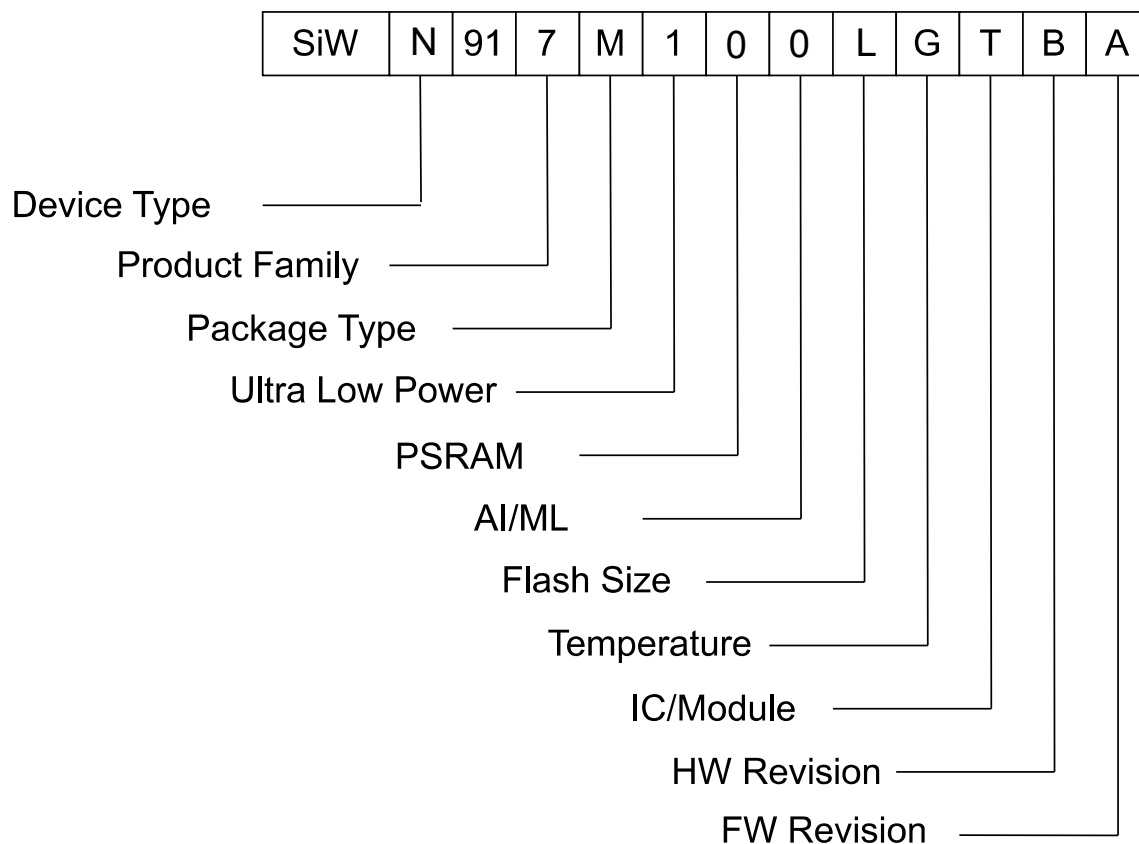| Part Number	Common Features	Device Type	Flash Size	Temperature
SiWN917M100XGTBA	Wi-Fi 6 Ultra low power IC, 7x7 QFN, Integrated 2.4 GHz Radio	NCP	No Stacked Flash	-40 to 85 ℃
SiWN917M100LGTBA		NCP	4MB Stacked Flash	-40 to 85 ℃

| SiW | N | 91 | 7 | M | 1 | 0 | 0 | L | G | T | B | A |

Device Type

Product Family

Package Type

Ultra Low Power

PSRAM

AI/ML

Flash Size

Temperature

IC/Module

HW Revision

FW Revision

Figure 2.1. Ordering Guide

Table 2.2. OPN Decoder

Field	Options
Device Type	**T**: RCP (Transceiver) **N**: NCP **G**: SoC
Product Family	**7**: Ultra-low power **5**: Ultra-low cost
Package Type	**M**: QFN

Field	Options
Ultra Low Power	**0**: ULP Features disabled
	1: ULP Features enabled
PSRAM	**0**: No PSRAM Support
	1: External PSRAM
	2: 2 MB Internal PSRAM
	4: 8 MB Internal PSRAM
AI/ML	**0**: AI/ML Features disabled
	1: AI/ML Features enabled
Flash Size	**X**: NO Internal Flash
	L: 4 MB Internal Flash
	M: 8 MB Internal Flash
Temperature	**G**: -40ºC to 85ºC
	N: -40ºC to 105ºC
IC/Module	**T**: IC Package
HW Revision	**B**: Revision B
FW Revision	**A**: Revision A

Table of Contents

3. Applications

Smart Home

Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs/switches, Light Emitting Diode (LED) lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

Other Consumer Applications

Toys, Anti-theft tags, Smart dispensers, Weighing scales, Fitness Monitors, Smart Glasses, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)

Healthcare Tags, Industrial Wearables, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, etc.

4. Block Diagrams

Figure 4.1. SiWN917 Hardware Block Diagram
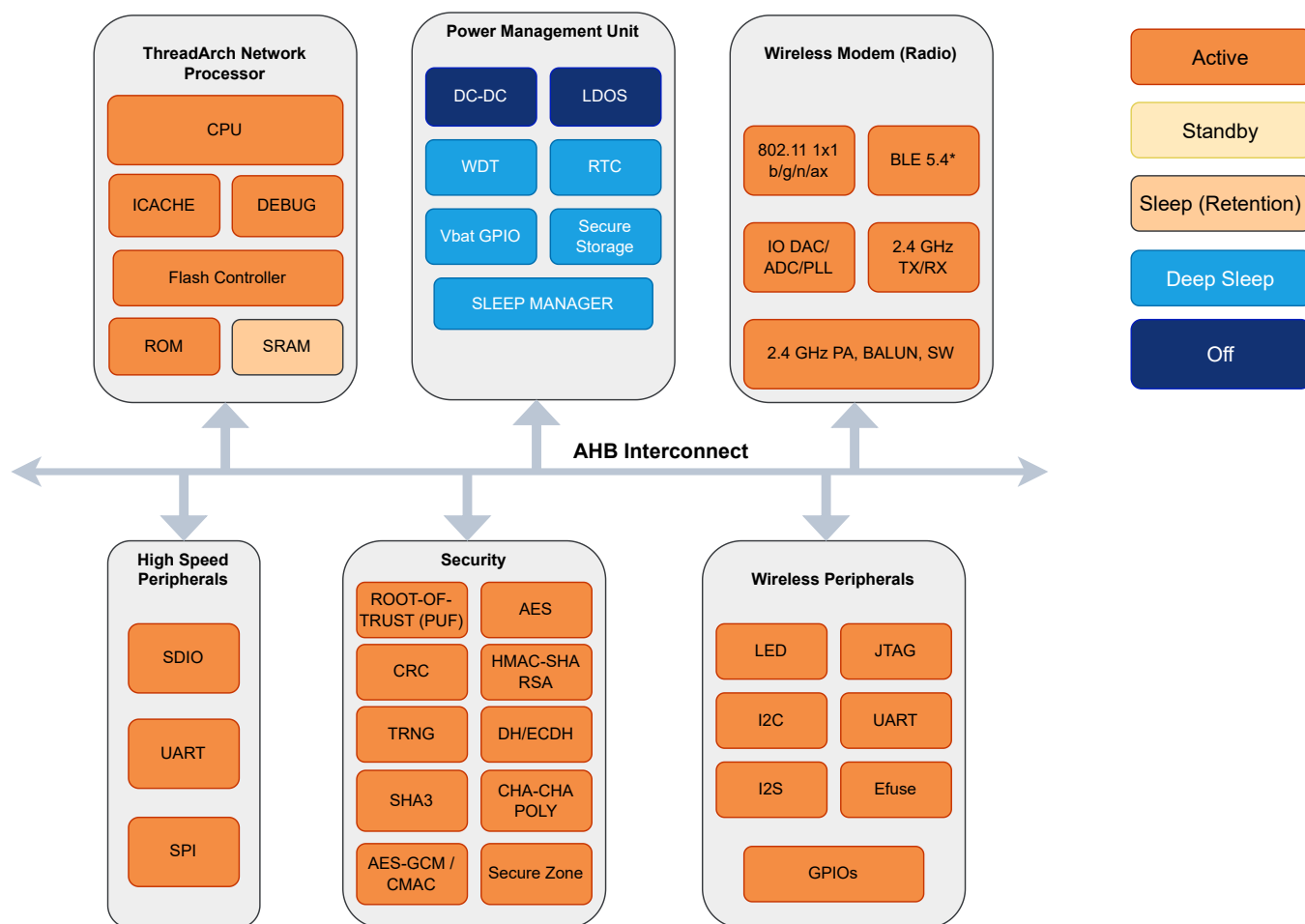
Figure 4.2. System Block Diagram
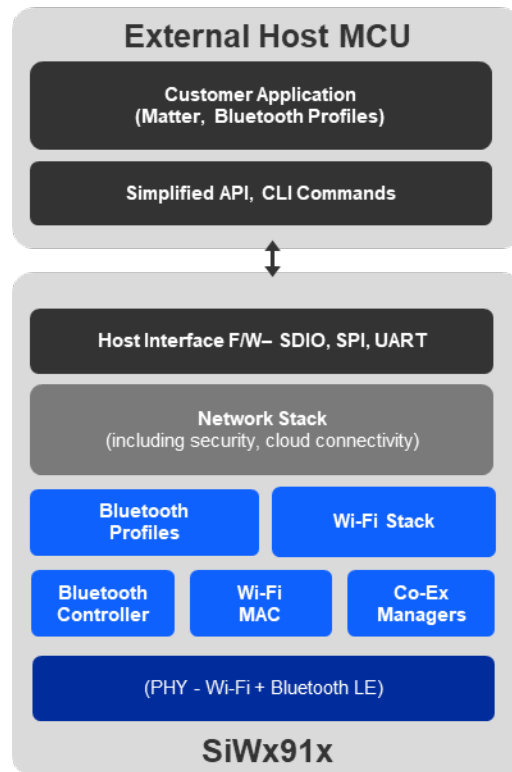
Figure 4.3. SiWN917 NCP Software Architecture

Note: Customer can connect multiple hosts, but only one host interface can be active after power-on.

5. System Overview

5.1 Introduction

SiWN91x NCP includes ThreadArch® 4-Threaded processor running up to 160MHz. All the networking and wireless stacks run on independent threads of the ThreadArch®. In addition, the ThreadArch® subsystem also acts as the secure processing domain and takes care of secure boot, secure firmware update and provides access to security accelerators and secure peripherals through pre-defined APIs. The ThreadArch® based "Networking, Security and Wireless subsystem" have power, clocks/PLLs, bus-matrices, and memory.

5.2 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
- Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
- Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi + BLE
- Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT),SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use, BSS Coloring, and NDP feedback up to 4 antennas
- Integrated PA
- Data Rates—802.11b: up to 11 Mbps; 802.11g: up to54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
- Operating Frequency Range: 2412 MHz – 2484 MHz

5.2.1 MAC

- Conforms to IEEE 802.11b/g/n/j/ax standards for MAC
- Hardware accelerators for AES
- WPA, WPA2, WPA3 and WMM support
- AMPDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS) and ECDH

5.2.2 Baseband Processing

- Supports 11b: DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11ax, 802.11n: MCS 0 to MCS 7
- High-performance multipath handling in OFDM, DSSS, and CCK modes

5.3 Bluetooth

Key Features
- Transmit power up to +20 dBm with integrated PA
- Receive sensitivity — LE: -95 dBm, LR 125 Kbps: -106 dBm
- Operating Frequency Range — 2.402 GHz - 2.480 GHz
- Support LE (1 Mbps & 2 Mbps) and LR (125 Kbps & 500 Kbps) rates
- Advertising extensions
- Data length extensions
- LL privacy
- LE dual role
- BLE acceptlist
- BLE 2 peripheral & 2 central connections or 1 central & 1 peripheral connection, 8 peripheral & 2 central
- BLE Mesh (4 nodes) for limited switch use case.

5.3.1 MAC

Link Manager
• Creation, modification & release of physical links
• Connection establishment between Link managers of two Bluetooth devices
• Link supervision is implemented in Link Manager
• Link power control is done depending on the inputs from Link Controller
• Enabling & disabling of encryption & decryption on logical links
• Support for security using AES hardware accelerator

Link Controller
• Encodes and decodes header of BLE packets
• Manages flow control, acknowledgment, re-transmission requests, etc.
• Stores the last packet status for all physical transports
• Indicates the success status of packet transmission to upper layers
• Indicates the link quality to the LMP layer

Device Manager
• Executes HCI Commands
• Controls Scan & Connection processes
• Controls all BLE Device operations except data transport operations
• BLE Controller state transition management
• Anchor point synchronization & management
• Scheduler

5.3.2 Baseband Processing

• Supports BLE 1Mbps, 2Mbps and long range 125kbps, 500kbps

5.4 RF Transceiver

• SiWx917 features two highly configurable RF transceivers supporting WLAN 11b/g/n/ax and Bluetooth LE wireless protocols. Both RF transceivers together operating in multiple modes covering High Performance (HP) and Low Power (LP) operations. List of operating modes are given in next section.
• It contains two fully integrated fractional-N frequency synthesizers having reference from internal oscillator with 40MHz crystal. One of the synthesizer is a low power architecture which also caters single-bit data modulation feature for Bluetooth LE protocols.
• There are two transmitter chains in the chip. First one uses a direct conversion architecture getting carrier signal from the high-performance frequency synthesizer. It contains an on-chip balun and its output is terminated as single-ended output at "RF_TX" pin. This transmitter supports all the mentioned WLAN protocols, and Bluetooth LE protocol for high output power. The second transmitter is a low power architecture for supporting constant envelope modulation formats. This has two outputs differentiated by their maximum output power level. The 0dBm output is shared with "RF_RX" pin and the 8 dBm output is terminated at "RF_BLETX" pin.
• The receiver contains two front end paths with a configurable common LNA catering HP and LP operations. This also has two analog base-band blocks where one is zero-IF architecture supporting all the mentioned WLAN protocols and the other one is low-IF architecture supporting Bluetooth LE. Input to the pin is "RF_RX" sharing with 0dBm Tx output.
• Impedance matching for each RF pins need to be done separately for optimum performance.

5.4.1 Receiver and Transmitter Operating Modes

The radio is highly configurable. The available radio operating modes are
• WLAN HP TX - WLAN High-Performance Transmitter
• WLAN HP RX - WLAN High-Performance Receiver
• WLAN LP RX - WLAN Low-Power Receiver
• BLE HP TX - Bluetooth LE High-Performance Transmitter
• BLE HP RX - Bluetooth LE High-Performance Receiver
• BLE LP TX - Bluetooth LE Low-Power Transmitter
• BLE LP RX - Bluetooth LE Low-Power Receiver

5.5 Security Features

- Secure Boot
- Secure OTA Firmware update
- TRNG : Generates high-entropy random numbers based on RF noise, increasing the effort/time needed to expose secret keys
- Secure Zone
- Secure Key storage : HW device identity and key storage with PUF
- Secure Debug
- Anti Rollback : Firmware downgrade to a lower version is prohibited through OTP to prevent the use of older, potentially vulnerable FW version
- Secure XIP from flash with XTS/CTR mode
- Secure Attestation : Allows a device to authenticate its identity using a cryptographically signed token and exchange of secret keys
- Hardware Accelerators: AES128/256/192, SHA256/384/512, HMAC, RNG, CRC, SHA3, AES-GCM/ CMAC, ChaCha-poly
- Software Accelerators: RSA and ECC
- Programmable Secure Hardware Write protect for Flash sectors

5.6 Embedded Wi-Fi Software

- The wireless software package supports Embedded Wi-Fi (802.11 b/g/n/ax) Client mode, Wi-Fi Access point mode (up to 4 clients), and Enterprise Security in client mode.
- The software package includes complete firmware and application profiles.
- It has a wireless coexistence manager to arbitrate between protocols.

5.6.1 Security

Wireless software supports multiple levels of security capabilities available for the development of IoT devices.
- Accelerators: AES128/256
- WPA/WPA2/WPA3-Personal, WPA/WPA2 Enterprise for Client

5.7 Power Architecture

The Power Control Hardware implements the control sequences for transitioning between different power states (Active/Standby/Sleep/Shutdown).

5.7.1 Highlights

- Two integrated buck switching regulators (High performance and ULP) to enable efficient Dynamic Voltage Scaling across wide operating mode currents ranging from <1μA to 300mA
- Multiple voltage domains with Independent voltage scaling of each domain.
- Fine grained power-gating including peripherals, buses and pads, thereby reducing power consumption when the peripheral/buses/pads are inactive.
- Flexible switching between different Active states with controls from Software.
- Hardware based wakeup from Standby/Sleep/Shutdown states.
- All the peripherals are clock gated by default thereby reducing the power consumption in inactive state.
- Low wakeup times as configurable by Software.

5.7.2 System Power Supply Configurations

SiWx917 chipsets support highly flexible power supply configurations for various application scenarios. Two application scenarios are listed below.
- 3.3 V single supply - A single 3.3 V supply derived from the system PMU can be input to all I/O supplies.
- 1.8 V and 3.3 V supply - A 1.8 V supply derived from the system PMU can be input to all I/O supplies except PA2G_AVDD. A 3.3 V supply derived from system Power Management Unit (PMU) can be fed to the power amplifier supply pin PA2G_AVDD. In this mode, I/Os can operate at 1.8 V without a penalty in the maximum transmit power

5.7.3 Power Management

The SiWx917 chipsets have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the chipset to operate from a wide variety of input sources.
- LC DC-DC switching converter for RF and digital blocks
  - Input voltage (1.8 V or 3.3 V) on pin VINBCKDC
  - Output - 1.45 V and 300 mA maximum load on pin VOUTBCKDC
- SC DC-DC - Switching converter for Always-ON core logic domain
  - Input voltage (1.8 V or 3.3 V) on pin UULP_VBATT_1 and UULP_VBATT_2
  - Output - 1.05 V
- SoC LDO - Linear regulator for digital blocks
  - Input - 1.45 V from LC DC-DC or external regulated supply on pin VINLDOSOC
  - Output - 1.15 V and 300 mA maximum load on pin VOUTLDOSOC
- LDO RF and AFE - Linear regulator for RF and AFE
  - Input - 1.45 V from LC DC-DC or external regulated supply on pin RF_AVDD
  - Output - 1.15 V and 20 mA maximum load on pin VOUTLDOAFE
- Flash LDO - Linear regulator for In-package flash and external flash
  - Input voltage (1.8 V or 3.3 V) on pin VINLDO1P8
  - Output - 1.8 V and 100 mA maximum load on pin VOUTLDO1P8

5.8 Memory Architecture

There are on chip Read Only Memory(ROM), Random Access Memory(RAM) and off chip FLASH connectivity. Sizes of ROM/RAM/FLASH will vary depending on the chip configuration.

The ThreadArch® processor has following memory:
- Embedded SRAM up to 672 kB total for ThreadArch®
- 448Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions
- 16Kbytes of Instruction cache (I cache) enabling eXecute In Place (XIP) with quad SPI flash memory.
- Flash up to 8 MB (embedded), up to 16 MB (External Flash)
- eFuse of 1024 bytes(used to store primary boot configuration, security and calibration parameters)

5.9 Low Power Modes

It supports Ultra-low power consumption with multiple power modes to reduce system energy consumption.
- Dynamic Voltage and Frequency Scaling
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to ULP mode.

5.9.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and TA processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 KHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:
- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

6. Pinout and Pin Description

6.1 Pin Diagram
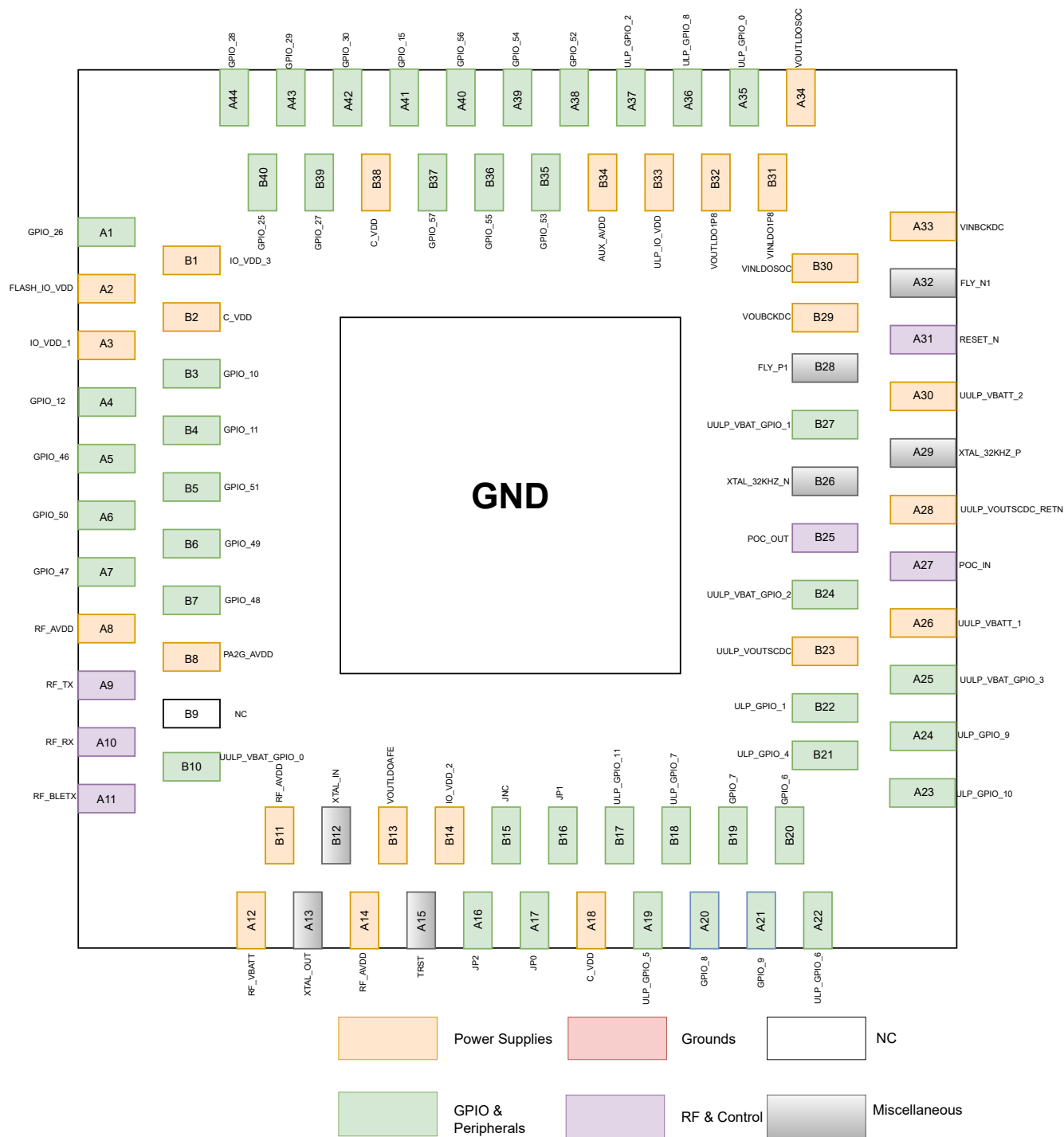
6.2 Pin Description

6.2.1 RF and Control Interfaces

Table 6.1. Chip Packages - RF and Control Interfaces

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RF_TX	A9	PA2G_AVDD	Output	NA	2.4 GHz RF Output.
RF_RX	A10	RF_AVDD	Inout	NA	2.4GHz RF Input for WLAN and BLE. It can also be used as BLE 0 dBm RF Output
RF_BLETX	A11	RF_AVDD	Output	NA	BLE 8 dBm RF Output
RESET_N	A31	UULP_VBATT_2	Input	NA	Active-low reset asynchronous reset signal. RESET_N will be pulled low if POC_IN is low.
POC_IN	A27	UULP_VBATT_1	Input	NA	This is an input to the chip. It should be made high only after supplies are valid to ensure the IC is in safe state until valid power supply is available.
POC_OUT	B25	UULP_VBATT_1	Output	NA	This is internally generated. Initially, it is low. But it becomes high when the supplies (UULP_VBATT_1, UULP_VOUTSCDC) are valid.
ULP_GPIO_0	A35	ULP_IO_VDD	Inout	NA	Antenna select pin for External switch configuration. Please refer to Reference schematics for more info.
ULP_GPIO_4	B21	ULP_IO_VDD	Inout	NA	Antenna select pin for External switch configuration.Please refer to Reference schematics for more info.
ULP_GPIO_5	A19	ULP_IO_VDD	Inout	NA	Antenna select pin for External switch configuration. Please refer to Reference schematics for more info.

6.2.2 Power and Ground Pins

Table 6.2. Chip Packages - Power and Ground Pins

Pin Name	Type	QFN Pin Number	Direction	Description
UULP_VBATT_1	Power	A26	Input	Always-on VBATT Power supply to the UULP domains.
UULP_VBATT_2	Power	A30	Input	Always-on VBATT Power supply to the UULP domains.
RF_VBATT	Power	A12	Input	Always-on VBATT Power supply to the RF.
VINBCKDC	Power	A33	Input	Power supply for the on-chip Buck.
VOUTBCKDC	Power	B29	Output	Output of the on-chip Buck.
VINLDOSOC	Power	B30	Input	Power supply for SoC LDO. Connect to VOUTBCKDC as per the Reference Schematics.
VOUTLDOSOC	Power	A34	Output	Output of SoC LDO.
VINLDO1P8	Power	B31	Input	Power supply for 1.8V LDO.
VOUTLDO1P8	Power	B32	Output	Output of 1.8V LDO which is used for Flash supply
VOUTLDOAFE	Power	B13	Output	Output of AFE LDO.
FLASH_IO_VDD	Power	A2	Input	I/O Supply for Flash. Connect to VOUTLDO1P8 as per the Reference Schematics.
IO_VDD_1	Power	A3	Input	I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
IO_VDD_2	Power	B14	Input	I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
IO_VDD_3 (SDIO_IO_VDD)	Power	B1	Input	I/O Supply for SDIO I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
ULP_IO_VDD	Power	B33	Input	I/O Supply for ULP GPIOs.
PA2G_AVDD	Power	B8	Input	Power supply for the 2.4 GHz RF Power Amplifier.
RF_AVDD	Power	A8, A14, B11	Input	Power supply for the 2.4 GHz RF and AFE. Connect to VOUTBCKDC as per the Reference Schematics.
AUX_AVDD	Power	B34	Output	Output supply for the Analog peripherals.
UULP_VOUTSCDC	Power	B23	Output	UULP Switched Cap DCDC Output.
UULP_VOUTSCDC_RETN	Power	A28	Output	UULP Retention Supply Output.
C_VDD	Power	B2, A18, B38	Input	Power supply for the digital core. Connect to the VOUTLDOSOC as per the Reference Schematics.
GND	Ground	GND Paddle	GND	Common ground pins.

6.2.3 Peripheral Interfaces

Table 6.3. Chip Packages - Peripheral Interfaces

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_6	B20	IO_VDD_1	Inout	HighZ	**Default:**HighZ **Sleep**: HighZ
GPIO_7	B19	IO_VDD_1	Inout	HighZ	**Default:**HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following. PTA_GRANT: "PTA Grant" output signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface.
GPIO_8/UART1_RX	A20	IO_VDD_1	Inout	HighZ	<table><tr><td>Host</td><td>Default</td><td>Sleep</td></tr><tr><td>UART</td><td>UART1_RX - UART Host interface serial input.</td><td>HighZ</td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table>
GPIO_9/UART1_TX	A21	IO_VDD_1	Inout	HighZ	<table><tr><td>Host</td><td>Default</td><td>Sleep</td></tr><tr><td>UART</td><td>UART1_TX - UART Host interface serial output.</td><td>HighZ</td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table>

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_10	B3	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep:** HighZ This pin can be configured by software to be any of the following. • HOST_WAKEUP_IND: This is used as indication from host to dev that host is ready to take the packet and device can transfer the packet to host. This is supported only in UART host mode. • It is part of Wake-on-Wireless functionality. Please check with Silabs for availability of this functionality
GPIO_11	B4	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep:** HighZ This pin can be configured by software to be any of the following. • WAKEUP_FROM_DEV: Used as a wakeup indication to host from device. • It is part of Wake-on-Wireless functionality. It is recommended that one use an external weak pull-down resistor on this pin and software has to be configured suitably. • Please check with Silabs for availability of this functionality.
GPIO_12	A4	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following. • UART1_RTS - UART interface Request to Send, if UART Host Interface flow control is enabled.
GPIO_15	A41	IO_VDD_3	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following. • UART1_CTS - UART interface Clear to Send, if UART Host Interface flow control is enabled.

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]		
GPIO_25/SDIO_CLK/ SPI_CLK	B40	IO_VDD_3	Inout	HighZ	Host	Default	Sleep
					SDIO	SDIO_CLK - SDIO interface clock	HighZ
					SPI	SPI_CLK - SPI Slave interface clock	HighZ
					Non SDIO,SPI	HighZ	HighZ
GPIO_26/SDIO_CMD/ SPI_CSN	A1	IO_VDD_3	Inout	HighZ	Host	Default	Sleep
					SDIO	SDIO_CMD - SDIO interface CMD signal	HighZ
					SPI	SPI_CSN - Active-low Chip Select signal of SPI Slave interface	HighZ
					Non SDIO,SPI	HighZ	HighZ
GPIO_27/SDIO_D0/ SPI_MOSI	B39	IO_VDD_3	Inout	HighZ	Host	Default	Sleep
					SDIO	SDIO_D0 - SDIO interface Data0 signal	HighZ
					SPI	SPI_MOSI - SPI Slave interface Master-Out-Slave-In signal	HighZ
					Non SDIO,SPI	HighZ	HighZ

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]		
GPIO_28/SDIO_D1/ SPI_MISO	A44	IO_VDD_3	Inout	HighZ	Host	Default	Sleep
					SDIO	SDIO_D1 - SDIO interface Data1 signal	HighZ
					SPI	SPI_MISO - SPI Slave interface Master-In- Slave-Out signal	HighZ
					Non SDIO,SPI	HighZ	HighZ
GPIO_29/SDIO_D2/ SPI_INTR	A43	IO_VDD_3	Inout	HighZ	Host	Default	Sleep
					SDIO	SDIO_D2 - SDIO interface Data2 signal	HighZ
					SPI	SPI_INTR - SPI Slave interface Interrupt Signal to the Host	HighZ
					Non SDIO,SPI	HighZ	HighZ
GPIO_30/SDIO_D3	A42	IO_VDD_3	Inout	Pullup	Host	Default	Sleep
					SDIO	SDIO_D3 - SDIO interface Data3 signal	HighZ
					Non SDIO,SPI	HighZ	HighZ
GPIO_46/QSPI_CLK	A5	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • QSPI_CLK - Clock to external Flash		

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_47/QSPI_D0	A7	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • QSPI_D0 - Data line to external flash
GPIO_48/QSPI_D1	B7	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • QSPI_D1 - Data line to external flash
GPIO_49/QSPI_CSN0	B6	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • QSPI_CSN0 - Chip select to external flash
GPIO_50/QSPI_D2	A6	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • QSPI_D2 - Data line to external flash
GPIO_51/QSPI_D3	B5	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • QSPI_D3 - Data line to external flash
GPIO_52	A38	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ
GPIO_53	B35	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ
GPIO_54	A39	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ
GPIO_55	B36	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ
GPIO_56	A40	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_57	B37	IO_VDD_1	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
ULP_GPIO_0	A35	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Antenna select pin for external switch configuration. Please refer to reference schematics for more info.
ULP_GPIO_1	B22	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • PTA_REQ: "PTA Request" input signal is part of 3-wire co-existence (Packet Traffic Arbitration) interface.
ULP_GPIO_2	A37	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
ULP_GPIO_4	B21	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Antenna select pin for external switch configuration. Please refer to reference schematics for more info.
ULP_GPIO_5	A19	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Antenna select pin for external switch configuration. Please refer to reference schematics for more info.
ULP_GPIO_6	A22	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following. • PTA_PRIO: "PTA Priority" input signal is part of 3-wire co-existence (Packet Traffic Arbitration) interface.
ULP_GPIO_7	B18	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
ULP_GPIO_8	A36	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
ULP_GPIO_9/ UART2_TX	A24	ULP_IO_VDD	Inout	HighZ	**Default:** UART2_TX- Debug UART Interface serial output **Sleep**: HighZ
ULP_GPIO_10	A23	ULP_IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ
ULP_GPIO_11	B17	ULP_IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep:** HighZ
UULP_VBAT_GPIO_0	B10	UULP_VBATT_1	Output	High	**Default:** EXT_PG_EN **Sleep:** EXT_PG_EN EXT_PG_EN: Reserved This pin can be configured by software to be any of the following. • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode.
UULP_VBAT_GPIO_1	B27	UULP_VBATT_1	Inout	HighZ	**Default:** HighZ **Sleep:** HighZ UULP_VBAT_GPIO_1: Reserved
UULP_VBAT_GPIO_2	B24	UULP_VBATT_1	Inout	HighZ	**Default:** HighZ **Sleep:** ULP_WAKEUP This pin can be configured by software to be any of the following. • HOST_BYP_ULP_WAKEUP: This signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from its Ultra Low Power (ULP) sleep mode.

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
UULP_VBAT_GPIO_3	A25	UULP_VBATT_1	Inout	HighZ	**Default:** HighZ **Sleep:** EXT_32KHZ_IN This pin can be configured by software to be any of the following. • EXT_32KHZ_IN: This pin can be used to feed external clock from a host processor or from external crystal oscillator.
JP0	A17	IO_VDD_2	Input	Pullup	**Default:** JP0 **Sleep**: HighZ JP0 - Reserved. Connect to a test point for debugging purposes
JP1	B16	IO_VDD_2	Input	Pullup	**Default:** JP1 **Sleep**: HighZ JP1 - Reserved. Connect to a test point for debugging purposes
JP2	A16	IO_VDD_2	Input	Pullup	**Default:** JP2 **Sleep**: HighZ JP2 - Reserved. Connect to a test point for debugging purposes
JNC	B15	IO_VDD_2	Output	Pullup	**Default:** JNC **Sleep**: HighZ JNC - Reserved. Connect to a test point for debugging purposes

Note:
1. "Default" state refers to the state of the device after initial boot loading and firmware loading is complete.
2. "Sleep" state refers to the state of the device after entering Sleep state
3. Please refer to "Hardware Reference Manual" for software programming information
4. Please refer to "Software Reference Manual" for software programming information
5. In the application, wherever SiWN917 is connected to an external host, during the power-off state, the host should ensure that all the pins (analog or digital) connected to the SiWN917 are not driven. Else, the pins must be grounded.

6.2.4 Miscellaneous Pins

Table 6.4. Miscellaneous Pins

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
FLY_P1	B28	NA	Input	NA	Fly Capacitor for Switched cap DCDC. Please refer to Reference Schematics

Pin Name	QFN Pin Number	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
FLY_N1	A32	NA	Input	NA	Fly Capacitor for Switched cap DCDC. Please refer to Reference Schematics
XTAL_IN	B12	RF_VBATT	Input	NA	Input to the on-chip oscillator from the external 40 MHz crystal.
XTAL_OUT	A13	RF_VBATT	Output	NA	Output of the on-chip oscillator to the external 40 MHz crystal.
TRST	A15	IO_VDD_2	Input	HighZ	Test signal. Connect to Ground.
XTAL_32KHZ_N	B26	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
XTAL_32KHZ_P	A29	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
NC	B9				No-Connect

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx

Note: All the specifications are preliminary and subject to change

Table 7.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
T_{store}	Storage temperature	-40	+125	ºC
$T_{j(max)}$	Maximum junction temperature	-	+125	ºC
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	-0.5	3.63	V
UULP_VBATT_2	Always-on VBATT supply to the UULP Domains	-0.5	3.63	V
RF_VBATT	Always-on VBATT Power supply to the RF	-0.5	3.63	V
VINBCKDC	Power supply for the on-chip Buck	-0.5	3.63	V
VINLDOSOC	Power supply for SoC LDO	-0.5	1.8	V
VINLDO1P8	Power supply for 1.8V LDO	-0.5	3.63	V
FLASH_IO_VDD	I/O supply for Flash	-0.5	3.63	V
IO_VDD_1	I/O supplies for GPIOs	-0.5	3.63	V
IO_VDD_2	I/O supplies for GPIOs	-0.5	3.63	V
IO_VDD_3	I/O supplies for GPIOs	-0.5	3.63	V
ULP_IO_VDD	I/O supplies for ULP GPIOs	-0.5	3.63	V
PA2G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	-0.5	3.63	V
RF_AVDD	Power supply for the 2.4 GHz RF and AFE	-0.5	1.98	V
C_VDD	Power supply for the digital core	-0.5	1.21	V
I_{max}	Maximum Current consumption in TX mode	-	400	mA
P_{max}	RF Power Level Input to the chip RF pins	-	10	dBm
I_{Pmax}	Total average max current into chip	-	500	mA

7.2 Recommended Operating Conditions

Table 7.2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{ambient}$	Ambient temperature	-40	25	85	ºC
$T_{junction}$	Junction temperature			105	ºC
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	1.71/2.97	1.8/3.3	1.98/3.63	V
UULP_VBATT_2	Always-on VBATT supply to the UULP Domains	1.71/2.97	1.8/3.3	1.98/3.63	V
RF_VBATT	Always-on VBATT Power supply to the RF	1.71/2.97	1.8/3.3	1.98/3.63	V
VINBCKDC	Power supply for the on-chip Buck	1.71/2.97	1.8/3.3	1.98/3.63	V
VINLDOSOC	Power supply for SoC LDO	1.35	1.45	1.55	V
VINLDO1P8	Power supply for 1.8V LDO	1.71/2.97	1.8/3.3	1.98/3.63	V
FLASH_IO_VDD	I/O supply for Flash	1.71	1.8	1.98	V
IO_VDD_1	I/O supply for GPIOs	1.71/2.97	1.8/3.3	1.98/3.63	V
IO_VDD_2	I/O supply for GPIOs	1.71/2.97	1.8/3.3	1.98/3.63	V
IO_VDD_3	I/O supply for GPIOs	1.71/2.97	1.8/3.3	1.98/3.63	V
ULP_IO_VDD	I/O supply for GPIOs	1.71/2.97	1.8/3.3	1.98/3.63	V
PA2G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	2.97	3.3	3.63	V

7.3 DC Characteristics

7.3.1 Reset Pin

Table 7.3. Reset Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage @3.3V	0.8 * UULP_VBATT_2	-		V
	High level input voltage @1.8V	1.17	-		V
V_{IL}	Low level input voltage @3.3V		-	0.3 * UULP_VBATT_2	V
	Low level input voltage @1.8V		-	0.63	V

7.3.2 Power On Control (POC) and Reset

The power on control has two control options. External source as input or internal loopback i.e. The POC_IN input of the chip can be connected to the internally generated POC_OUT signal. RESET_N will be pulled low if POC_IN is low.

7.3.2.1 POC_OUT Connected to POC_IN

The IC generates a POC (Power On Control) signal - POC_OUT that is distributed to all I/O cells to prevent the I/O cells from powering up in an undesired configuration and is also used inside the IC to safe state the IC till a valid supply is available for proper operation. This power management is functional in both power up and power down sequences.

During power up, until the UULP_VBATT_1 and UULP_VBATT_2 (VBATT supply) reach 1.6V, the POC_OUT signal stays low. Once the VBATT supply exceeds 1.6V, the POC_OUT becomes high and normal operation of the IC starts.

Once the POC_OUT becomes high, it stays high. But if VBATT becomes lower than the Blackout threshold voltage, POC_OUT becomes low

The following figure illustrates the power up sequence when POC_OUT is connected to POC_IN. As shown in the figure below, the RESET_N is high at least 1.6ms after VBATT supply is stable. The RESET_N signal can be controlled via options like an R/C circuit or another MCU's GPIO.
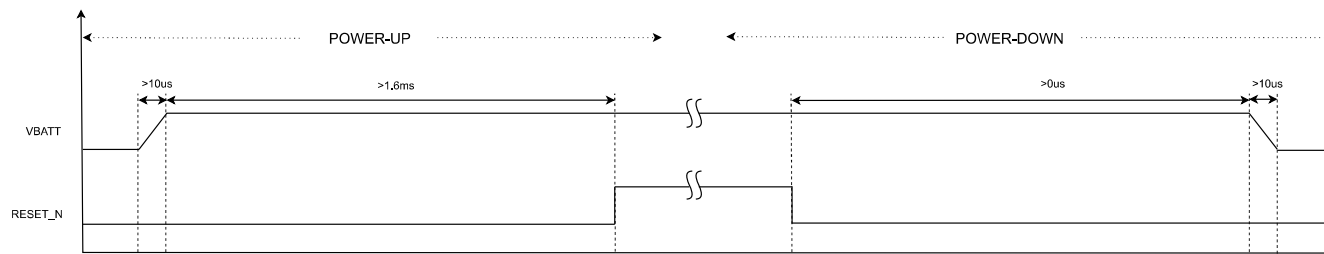
Figure 7.1. Power Up Sequence when POC_OUT is Connected to POC_IN

7.3.2.2 External Control for POC_IN

The POC_IN and RESET_N signals can be controlled from external source like R/C circuits and/or another MCU's GPIOs . The figure below illustrates the requirement for controlling POC_IN and RESET_N with respect to the VBATT supplies.
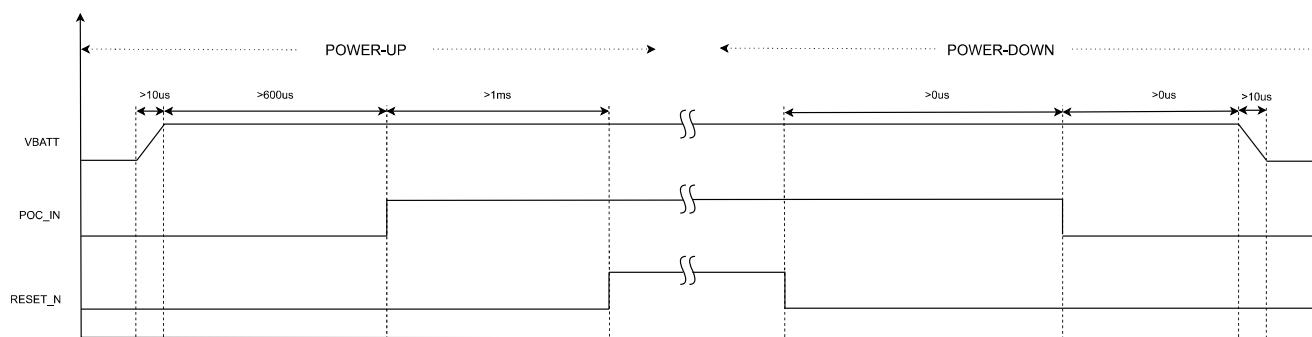
Figure 7.2. Power Up Sequence with External Control for POC_IN

7.3.3 ULP Regulator

ULP (Ultra Low Power) regulators are used to power low power Always-ON (AON) digital and analog power management circuitry inside the IC. The ULP regulators include two high power LDOs , a Low power LDO, and a switched capacitor DC-DC regulator. These regulators operate directly off of UULP_VBATT_2 (VBATT supply).

7.3.3.1 Block Diagram
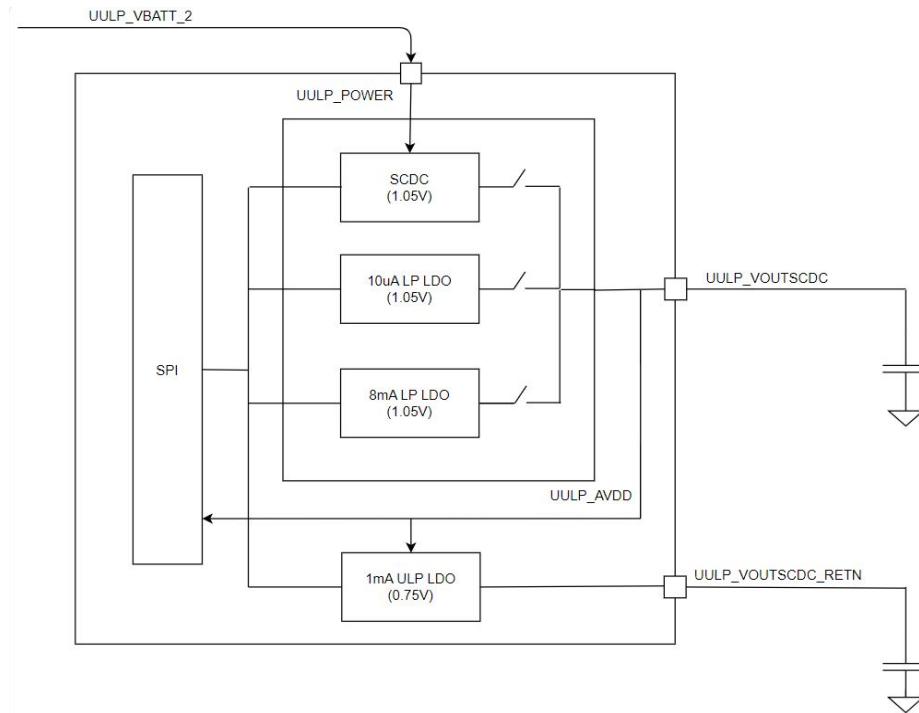
7.3.3.2 SC-DCDC

SC-DCDC stands for a Switched Capacitor DC-DC regulator. It operates from VBATT and generates a programmable output voltage. It has two major modes of operation, viz. LDO mode and DC-DC mode. And further each of these modes have a low power and high power option.

The IC starts up in the LDO mode and later switches to DC-DC Mode..

SC-DCDC

Table 7.4. SC-DCDC - Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V_{in}	Input Voltage Range		1.71		3.63	V
Note: The ULP regulator switches from SC-DCDC mode to LDO mode for V_{in} lower than 2.4V						

7.3.4 SoC Power Management Unit

This section describes and specifies the Power Management Unit solution for the mixed signal System on Chip (SoC).
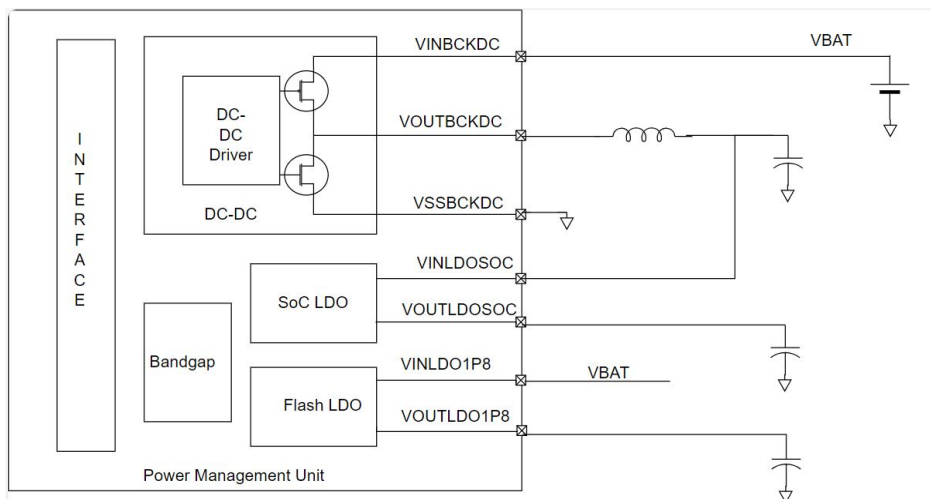
Power Management Unit

The major features are

- 1.45V DCDC switching converter
- 1.15V LDO for SOC digital supply
- 1.8V LDO for Flash supply

7.3.4.1 DCDC Switching Converter

- Power save mode at light load currents.
- 100% duty cycle for lowest dropout.
- Soft start

Table 7.5. DCDC Switching Converter Electrical Specifications

Parameter	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{in}	Input Supply Voltage (VINBCKDC)		1.71	3.3	3.63	V
V_{out}	Output Voltage Range (VOUTBCKDC)		TBD	1.45	TBD	V
I_{load}	Load current	Active mode			250	mA

7.3.4.2 SoC LDO

Table 7.6. SoC LDO Electrical Specifications

Parameter	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{in}	Input Supply Voltage (VINLDOSOC)		1.35	1.45	1.55	V
V_{out}	Output Voltage Range (VOUTLDO-SOC)		TBD	1.15	TBD	V
I_{load}	Load current				200	mA

7.3.4.3 Flash LDO

Table 7.7. Flash LDO Electrical Specifications - Regulation Mode

Parameter	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{in}	Input Supply Voltage (VINLDO1P8)	Flash LDO in Regulation Mode	2.97	3.3	3.63	V
V_{out}	Output Voltage (VOUTLDO1P8)		TBD	1.8	TBD	V
I_{load}	Load current				48.00	mA
Line Regulation		V_{in} Changed from 2.97V to 3.63V			0.60	%
Load Regulation		I_{load} changed from 0mA to 48mA			1.40	%

Table 7.8. Flash LDO Electrical Specifications - Bypass Mode

Parameter	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{in}	Input Supply Voltage (VINLDO1P8)	Flash LDO in Bypass Mode	TBD	1.8	1.98	V
R_{on}	On Resistance between V_{in} and V_{out}			0.87		Ohm
V_{drop}	Voltage across the V_{in} and V_{out} pin of the Flash LDO	Load = 48mA (Max)		42		mV
V_{out}	Flash Output Voltage	Load = 48mA at V_{in} = 1.71V	TBD	1.67		V
		Load = 48mA at V_{in} = 1.75V	TBD	1.71		V

Note: For Higher load currents, the input supply should be increased to compensate the V_{drop} across the R_{on} of the Pass transistor of Flash LDO.

7.3.5 Thermal Characteristics

Table 7.9. Thermal Characteristics

Package	Board	Parameter	Symbol	Test Condition	Value	Unit
84 Pin DR-QFN (7mm x 7mm)	JEDEC - High Thermal Cond. (2s2p)[1]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	30	°C/W

Note:
  1. PCB: 76.2mm x 114.3mm x 1.6mm (JEDEC High Effective); 2s2p = 2 signals, 2 planes.

7.3.6 Digital Input Output Signals

Table 7.10. Digital I/O Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage @ IO_VDDx = 3.3V	2.0	-	-	V
	High level input voltage @ IO_VDDx = 1.8V	1.17	-	-	V
V_{IL}	Low level input voltage @ IO_VDDx = 3.3V	-	-	0.8	V
	Low level input voltage @ IO_VDDx = 1.8V	-	-	0.63	V
V_{OL}	Low level output voltage	-	-	0.4	V
V_{OH}	High level output voltage	IO_VDDx -0.4	-	-	V
I_{OL}	Low level output current	2.0	4.0	12.0	mA
I_{OH}	High level output current	2.0	4.0	12.0	mA
$I_{OL\ for\ UULP\_GPIO\_*}$	Low level output current	1.0		2.0	mA
$I_{OH\ for\ UULP\_GPIO\_*}$	High level output current	1.0		2.0	mA

7.3.6.1 Open-Drain I2C Pins

Table 7.11. Open-Drain I2C Pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage	0.7 * IO_VDDx	-	-	V
V_{IL}	Low level input voltage	-	-	0.3 * IO_VDDx	V

7.4 AC Characteristics

7.4.1 Clock Specifications

SiWx917 chipsets require two primary clocks:
- Low frequency 32 kHz clock for sleep manager and RTC
  - Internal 32 kHz RC clock is used for applications with low timing accuracy requirements
  - 32 kHz external crystal clock is used for applications with high timing accuracy requirements
- High frequency clocks
  - 40 MHz Ref clock
  - 32 MHz RC clock
  - High frequency ring oscillator

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where an external clock source is already present, the clock can be reused.

32 kHz XTAL sources:
- External XTAL oscillator providing LVCMOS rail to rail clock input on UULPGPIO (Nano-drive clock should not be supplied).
- Internal 32KHz crystal oscillator.

7.4.1.1 32 kHz Clock

7.4.1.2 Low Frequency Clocks

The 32 kHz clock selection can be done through software. RC oscillator clock is not suited for high timing accuracy applications and can increase system current consumption in duty-cycled power modes.

32 kHz RC Oscillator

Table 7.12. 32 kHz RC Oscillator

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		32.0		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage		1.2		%

32 kHz External Oscillator

An external 32 kHz low-frequency clock can be fed through UULP GPIO.
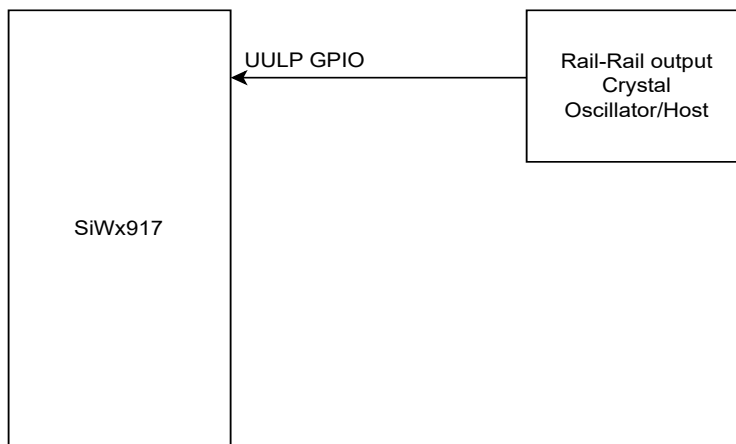
Figure 7.3. External 32 kHz Oscillator - Rail to Rail

Table 7.13. 32 kHz External Oscillator Specifications

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		32.768		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-100		100	ppm
Duty cycle	Input duty cycle	30	50	70	%
V_{AC}	Input AC peak-peak voltage swing at input pin.	-0.3	-	VBATT +/- 10%	Vpp

32 kHz Internal XTAL Oscillator

There is an option to use internal 32 kHz low-frequency XTAL clock. Below are the recommended external crystal specs that need to connect to the internal xtal oscillator.
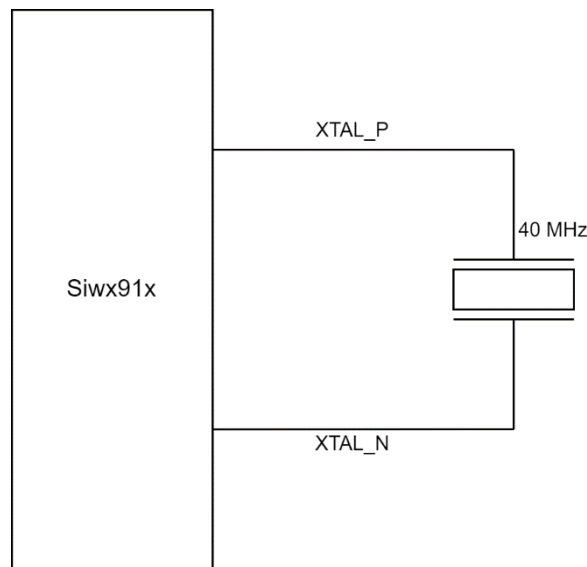
Table 7.14. Internal 32 kHz XTAL Oscillator

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		32.768		kHz
Mode	Mode of Operation	Fundamental			
Resonance	Series or Parallel Resonance	Parallel			
Drive	Drive Level	0.5			uW
F_{osc_Acc}	Frequency Stability *		+/- 250		ppm
ESR	Equivalent series resistance			80	KΩ
Load cap	Load capacitance range	4		12.5	pF

Note: Combined frequency offset must be below this limit, with temperature induced changes, tolerance, and the variance of load capacitances (load capacitor and parasitic trace impedance)

7.4.1.3 40 MHz Clock

The 40 MHz internal oscillator mode can be used by connecting a 40 MHz crystal between the pins XTA L_P and XTAL_N. Load capacitance is integrated inside the chipset and calibrated and the calibrated value can be stored in eFuse using calibration software.

Table 7.15. 40 MHz Crystal Specifications

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		40		MHz
Mode	Mode of Operation	Fundamental			
Resonance	Series or Parallel Resonance	Parallel			
Drive	Drive Level	100			uW
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-20		20	ppm
ESR	Equivalent series resistance			60	Ω
Load cap	Load capacitance range	7		10	pF

7.4.1.4 32 MHz RC Oscillator

Table 7.16. 32 MHz RC Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
F_{osc}	Oscillation Frequency	Trimmed Frequency		31.7		MHz

7.4.2 SDIO 2.0 Secondary

7.4.2.1 Full Speed Mode

Table 7.17. AC Characteristics - SDIO 2.0 Secondary Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{sdio}	SDIO_CLK	-	-	25	MHz
T_s	SDIO_DATA, SDIO_CMD input setup time	4	-	-	ns
T_h	SDIO_DATA, SDIO_CMD input hold time	1.2	-	-	ns
T_{od}	SDIO_DATA, clock to output delay	-	-	13	ns
C_L	Output Load	5	-	10	pF

Figure 7.4. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode

7.4.2.2 High Speed Mode

Table 7.18. AC Characteristics - SDIO 2.0 Secondary High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{sdio}	SDIO_CLK	25	-	50	MHz
T_s	SDIO_DATA, input setup time	4	-	-	ns
T_h	SDIO_DATA, input hold time	1.2	-	-	ns
T_{od}	SDIO_DATA, clock to output delay	2.5	-	13	ns
C_L	Output Load	5	-	10	pF

Figure 7.5. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode

7.4.3 SPI Secondary

7.4.3.1 Low Speed Mode

Table 7.19. AC Characteristics - SPI Secondary Low Speed Mode

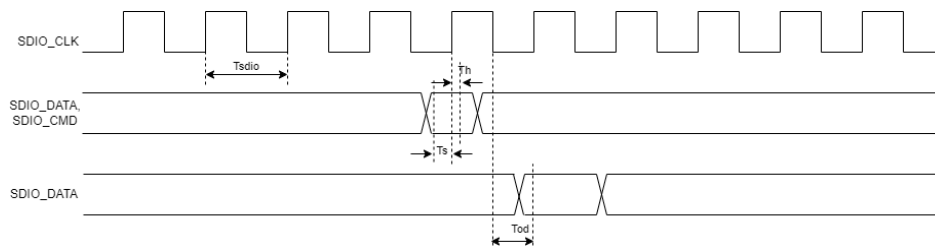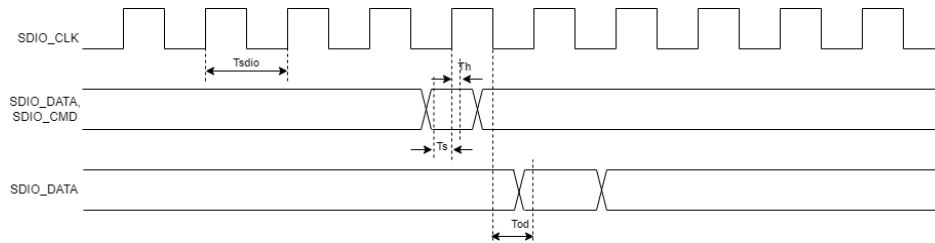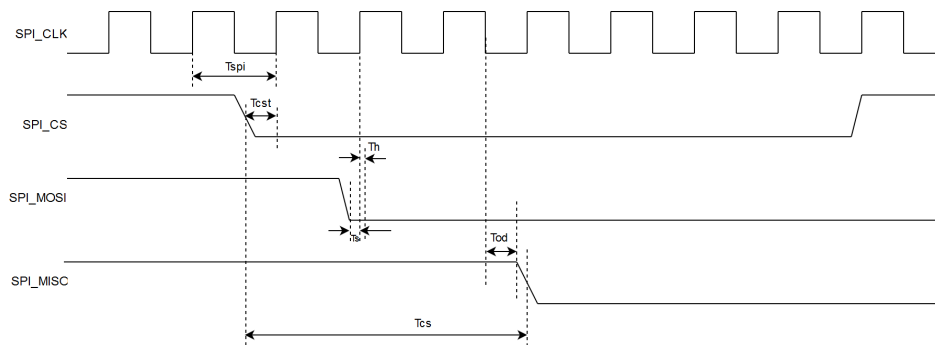| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	0	-	25	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.4	-	-	ns
T_h	SPI_MOSI, input hold time	1.5	-	-	ns
T_{od}	SPI_MISO, clock to output delay	-	-	8.75	ns
C_L	Output Load	5	-	10	pF

Figure 7.6. Interface Timing Diagram for SPI Secondary Low Speed Mode

7.4.3.2 High Speed Mode

Table 7.20. AC Characteristics - SPI Secondary High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	25	-	80	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.4	-	-	ns
T_h	SPI_MOSI, input hold time	1.4	-	-	ns
T_{od}	SPI_MISO, clock to output delay	1.5	-	8.75	ns
C_L	Output Load	5	-	10	pF
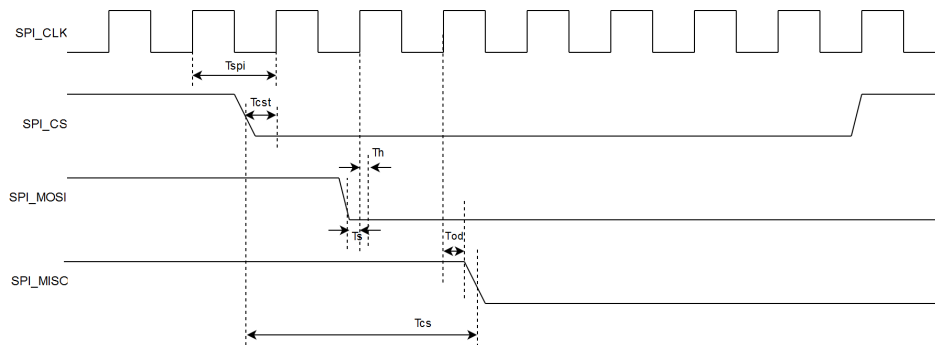
Figure 7.7. Interface Timing Diagram for SPI Secondary High Speed Mode

7.4.3.3 Ultra High Speed Mode

Table 7.21. AC Characteristics - SPI Secondary Ultra High Speed Mode

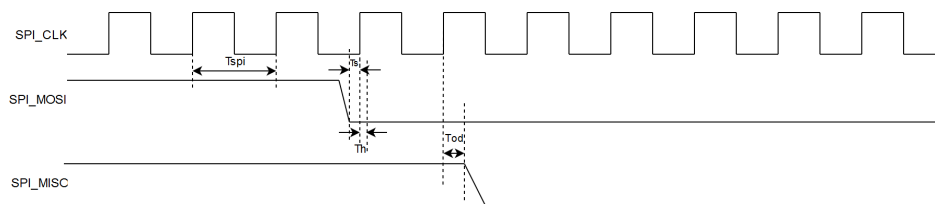| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	80	-	100	MHz
T_s	SPI_MOSI, input setup time	1.4	-	-	ns
T_h	SPI_MOSI, input hold time	1.4	-	-	ns
T_{od}	SPI_MISO, clock to output delay	1.5	-	8.75	ns
C_L	Output Load	5	-	10	pF

Figure 7.8. Interface Timing Diagram for SPI Secondary Ultra High Speed Mode

7.4.4 UART

Table 7.22. AC Characteristics - UART

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{uart}	CLK	0	-	20	MHz
T_{od}	Output delay	0	-	10	ns
C_L	Output load	5	-	25	pF

7.4.5 GPIO Pins

Table 7.23. AC Characteristics - GPIO Pins

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
T_{rf}	Rise time	Pin configured as output; SLEW = 1(fast mode)	1.0	-	4	ns
T_{ff}	Fall time	Pin configured as output; SLEW = 1(fast mode)	0.9	-	4	ns
T_{rs}	Rise time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	5	ns
T_{fs}	Fall time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	5	ns
T_r	Rise time	Pin configured as input	0.3	-	1.3	ns
T_f	Fall time	Pin configured as input	0.2	-	1.2	ns

7.4.6 Flash Memory

Table 7.24. AC Characteristics - Flash Memory

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
N_{endu}	Endurance	Sector erase/program	10000	-	-	cycles
		Page erase/program, page in large sector	10000	-	-	cycles
		Page erase/program, page in small sector	10000	-	-	cycles
T_{ret}	Retention time	Powered	10	-	-	years
		Unpowered	10	-	-	years
T_{er}	Block Erase time (32KB)	Page, sector or multiple consecutive sectors	-	150	1400	ms
T_{prog}	Page Programming time		-	0.5	3	ms
T_{ce}	Chip Erase time			20	65	s

7.4.7 I2C

7.4.7.1 Fast Speed Mode

Table 7.25. AC Characteristics - I2C Fast Speed Mode

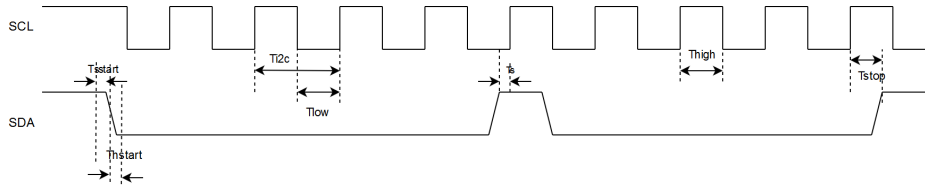| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	100	-	400	KHz
T_{low}	clock low period	1.3	-	-	us
T_{high}	clock high period	0.6	-	-	us
T_{sstart}	start condition, setup time	0.6	-	-	us
T_{hstart}	start condition, hold time	0.6	-	-	us
T_s	data, setup time	100	-	-	ns
T_{sstop}	stop condition, setup time	0.6	-	-	us
C_L	Output Load	5	-	10	pF

Figure 7.9. Interface Timing Diagram for I2C Fast Speed Mode

7.4.7.2 High Speed Mode

Table 7.26. AC Characteristics - I2C High Speed Mode

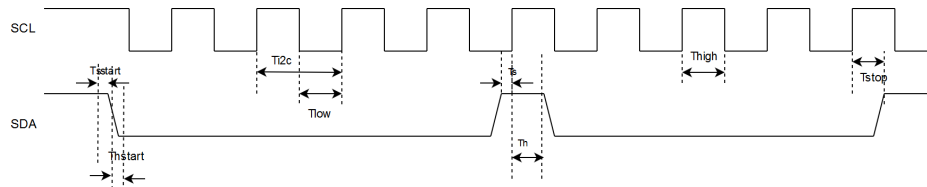| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	0.4	-	3.4	MHz
T_{low}	clock low period	160	-	-	ns
T_{high}	clock high period	60	-	-	ns
T_{sstart}	start condition, setup time	160	-	-	ns
T_{hstart}	start condition, hold time	160	-	-	ns
T_s	data, setup time	10	-	-	ns
T_h	data, hold time	0	-	70	ns
T_{sstop}	stop condition, setup time	160	-	-	ns
C_L	Output Load	5	-	10	pF

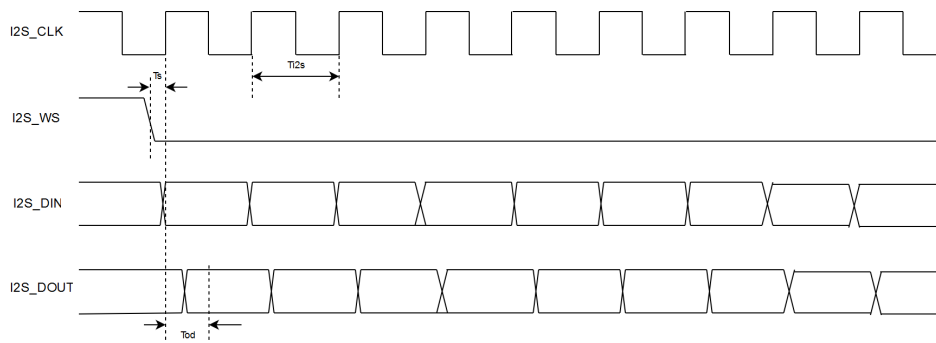**Figure 7.10. Interface Timing Diagram for I2C High Speed Mode**

7.4.8 I2S/PCM Primary and Secondary

7.4.8.1 Primary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Table 7.27. AC Characteristics – I2S/PCM Primary Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	10	-	-	ns
T_h	i2s_din,i2s_ws hold time	3	-	-	ns
T_{od}	i2s_dout output delay	0	-	15	ns
C_L	i2s_dout output load	5	-	10	pF

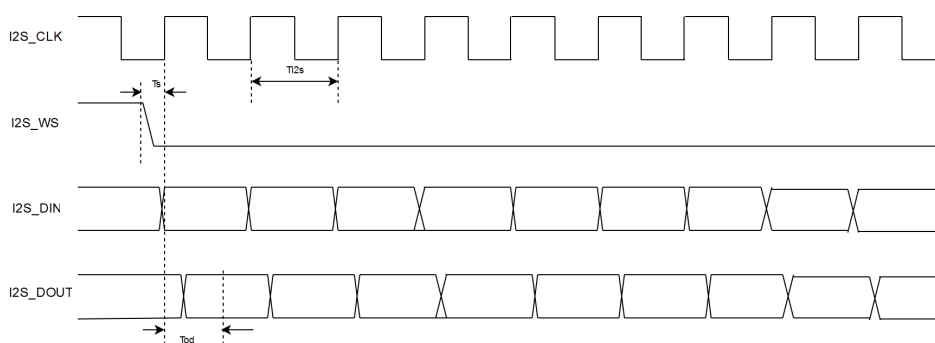**Figure 7.11. Interface Timing Diagram for I2S Primary Mode**

7.4.8.2 Secondary Mode

Negedge driving and posedge sampling for I2S

Posedge driving and negedge sampling for PCM

Table 7.28. AC Characteristics - I2S/PCM Secondary Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	7.5	-	-	ns
T_h	i2s_din,i2s_ws hold time	2	-	-	ns
T_{od}	i2s_dout output delay	0	-	17	ns
C_L	i2s_dout output load	5	-	10	pF

Figure 7.12. Interface Timing Diagram for I2S Secondary Mode

7.5 RF Characteristics

In the sub-sections below,

- All numbers are measured at Typical operating conditions (TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V) unless otherwise stated. For Support of 1.8 V on RF/PA, please contact Silicon Labs.
- Please refer to Section 8.1.1 (Reference Schematics). As shown in Reference Schematics (RF Front End-External Switch), there are "3" IC Pins "RF_TX, RF_RX, and RF_BLE_TX". RF Front end includes the matching network, RF switch and a band-pass filter. Typical Front-end loss is about 2-dB. Silicon Labs recommends using suggested reference design to be able to meet these specs.
- In the sub-sections below, all reported Receiver Sensitivity and Transmit Power numbers are at IC pins based on RF Front End (External Switch option). The value at the antenna port will be based on Front End loss (Typically 2dB lower than at IC pin)
- Following performance numbers are measured at Typical and room temperature operating conditions. There can be variation across parts and PVT.

7.5.1 WLAN 2.4 GHz Transmitter Characteristics

7.5.1.1 Transmitter Characteristics with 3.3V Supply

• TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_TX).

Table 7.29. Transmitter Characteristics with 3.3 V Supply

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 20MHz Bandwidth, with EVM limits	DSSS - 1 Mbps	EVM< -9 dB	-	20	-	dBm
	CCK - 11 Mbps	EVM< -9 dB	-	20	-	dBm
	OFDM - 6 Mbps	EVM< -5 dB	-	20	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB	-	16	-	dBm
	HT MCS0 Mixed Mode	EVM< -5 dB	-	20	-	dBm
	HT MCS7 Mixed Mode	EVM< -27 dB	-	15.5	-	dBm
	HE MCS0 SU	EVM< -5 dB	-	18.5	-	dBm
	HE MCS7 SU	EVM< -27 dB	-	14	-	dBm

Note:

1. There can be a variation of up to 2dB in Tx power across channels at Typical/Room temperature.

2. Each device is tested during manufacturing and set for best power while meeting the IEEE EVM and spectral mask requirements. It is mandatory for the customer to calibrate Crystal ppm offset error and recommended to adjust Gain offset on their hardware to achieve accurate Tx power for regulatory purposes. Refer to App notes for more details.

3. To meet FCC emission limits, Band-Edge channels (1 and 11) Tx Power will be lowest .Other Channels will be relatively lower compared to middle channels. Refer to Regulatory Certification App note for more details. The radiated power in band edge is a strong function of the antenna properties. Front end reference design has an external bandpass filter to meet the regulatory emission standards, including FCC. Silicon Labs recommends using the same reference design.

4. Channels 1 (2412 MHz) through 11 (2462 MHz) are supported for FCC. Channels 1 (2412 MHz) through 13 (2472MHz) are supported for Europe and Japan. Channel 14 is supported for Japan.

7.5.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) RF Chain

- TA = 25°C,PA2G_AVDD/VINBCKDC= 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_RX)
- All WLAN receiver sensitivity numbers and adjacent channel numbers are at < 10% PER limit for 11g/n/ax rates and <8% PER limit for 11b rates
  - Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11n
  - Packet sizes are 4096 bytes for 802.11ax for SU
- Carrier modulation is non-DCM
- For WLAN ACI cases, the desired signal power is 3 dB (11g/n/ax) and 6dB (11b) above standard defined sensitivity levels respectively

Table 7.30. WLAN 2.4 GHz Receiver Characteristics on HP RF Chain

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth[1]	11b 1 Mbps DSSS	-	-97.5	-	dBm
	11b 2 Mbps DSSS	-	-92.5	-	dBm
	11b 5.5 Mbps CCK	-	-91	-	dBm
	11b 11 Mbps CCK	-	-88	-	dBm
	11g 6 Mbps OFDM	-	-93	-	dBm
	11g 9 Mbps OFDM	-	-92	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-86	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-78	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
	HT MCS0 Mixed Mode	-	-92	-	dBm
	HT20 MCS1 Mixed Mode	-	-90.5	-	dBm
	HT20 MCS2 Mixed Mode	-	-87.5	-	dBm
	HT20 MCS3 Mixed Mode	-	-85	-	dBm
	HT20 MCS4 Mixed Mode	-	-81	-	dBm
	HT20 MCS5 Mixed Mode	-	-77	-	dBm
	HT20 MCS6 Mixed Mode	-	-75	-	dBm
	HT20 MCS7 Mixed Mode	-	-73	-	dBm
	HE20 MCS0 SU	-	-91.5	-	dBm
	HE20 MCS1 SU	-	-90	-	dBm
	HE20 MCS2 SU	-	-87	-	dBm
	HE20 MCS3 SU	-	-84.5	-	dBm
	HE20 MCS4 SU	-	-80.5	-	dBm
	HE20 MCS5 SU	-	-76.5	-	dBm
	HE MCS6 SU	-	-74.5	-	dBm
	HE MCS7 SU	-	-72	-	dBm
	HE MCS0 ER	-	-92.5	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	3	-	dBm
	802.11g	-	-2	-	dBm
	802.11n	-	-4	-	dBm
	802.11ax	-	-2.5	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
Adjacent Channel Interference	1 Mbps DSSS	-	43	-	dB
	11 Mbps DSSS	-	35	-	dB
	6 Mbps OFDM	-	38	-	dB
	54 Mbps OFDM	-	18	-	dB
	HT MCS0 Mixed Mode	-	38	-	dB
	HT MCS7 Mixed Mode	-	17	-	dB
	HE MCS0 SU	-	16	-	dB
	HE MCS7 SU	-	3	-	dB
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	49	-	dB
	11 Mbps DSSS	-	42	-	dB
	6 Mbps OFDM	-	49	-	dB
	54 Mbps OFDM	-	27	-	dB
	HT MCS0 Mixed Mode	-	48	-	dB
	HT MCS7 Mixed Mode	-	26	-	dB
	HE MCS0 SU	-	48	-	dB
	HE MCS7 SU	-	25	-	dB

Note:
1. Rx Sensitivity Variation is up to 1 dB for channels (1, 2, 3, 4, 5, 9, and 10) at Typical/Room temperature.
2. Rx sensitivity may be degraded up to 2 dB for channels (6, 7, 8, 11, 12, 13, and 14) at Typical/Room temperature.

7.5.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) RF Chain

- TA = 25°C,PA2G_AVDD/VINBCKDC= 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_RX)
- All WLAN receiver sensitivity numbers and adjacent channel numbers are at < 10% PER limit for 11g/n/ax rates and <8% PER limit for 11b rates
  - Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11n
  - Packet sizes are 4096 bytes for 802.11ax for SU
- Carrier modulation is non-DCM
- For WLAN ACI cases, the desired signal power is 3 dB (11g/n/ax) and 6dB (11b) above standard defined sensitivity levels respectively

Table 7.31. WLAN 2.4 GHz Receiver Characteristics on LP RF Chain

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth[1]	11b 1 Mbps DSSS	-	-97	-	dBm
	11b 2 Mbps DSSS	-	-92	-	dBm
	11b 5.5 Mbps CCK	-	-90.5	-	dBm
	11b 11 Mbps CCK	-	-87.5	-	dBm
	11g 6 Mbps OFDM	-	-92.5	-	dBm
	11g 9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-90.5	-	dBm
	18 Mbps OFDM	-	-88.5	-	dBm
	24 Mbps OFDM	-	-85.5	-	dBm
	36 Mbps OFDM	-	-81.5	-	dBm
	HT20 MCS0 Mixed Mode	-	-91.5	-	dBm
	HT20 MCS1 Mixed Mode	-	-90	-	dBm
	HT20 MCS2 Mixed Mode	-	-87	-	dBm
	HT20 MCS3 Mixed Mode	-	-84.5	-	dBm
	HT20 MCS4 Mixed Mode	-	-80.5	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	-6	-	dBm
	802.11g	-	0.5	-	dBm
	802.11n	-	-0.5	-	dBm
	802.11ax	-	-	-	dBm
Adjacent Channel Interference	1 Mbps DSSS	-	43	-	dB
	11 Mbps DSSS	-	36	-	dB
	6 Mbps OFDM	-	38	-	dB
	36 Mbps OFDM	-	25	-	dB
	HT MCS0 Mixed Mode	-	38	-	dB
	HT MCS4 Mixed Mode	-	24	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Units
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	46	-	dB
	11 Mbps DSSS	-	40	-	dB
	6 Mbps OFDM	-	43	-	dB
	36 Mbps OFDM	-	31	-	dB
	HT MCS0 Mixed Mode	-	43	-	dB
	HT MCS4 Mixed Mode	-	30	-	dB

Note:

1. Rx Sensitivity Variation is up to 1 dB for channels (1, 2, 3, 4, 5, 9, and 10) at Typical/Room temperature.
2. Rx sensitivity may be degraded up to 2 dB for channels (6, 7, 8, 11, 12, 13, and 14) at Typical/Room temperature.

7.5.4 Bluetooth Transmitter - Characteristics on High-Performance (HP) RF Chain

7.5.4.1 Transmitter Characteristics with 3.3 V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_TX)

Table 7.32. Bluetooth Transmitter Characteristics with 3.3 V Supply

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power	LE 1Mbps		-	19.5	-	dBm
	LE 2Mbps		-	19.5	-	dBm
	LR 500 Kbps		-	19	-	dBm
	LR 125 Kbps		-	19.5	-	dBm
Adjacent Channel Power |M-N| = 2	LE		-	-26	-	dBm
	LR		-	-	-	dBm
Adjacent Channel Power |M-N| > 2	LE		-	-36	-	dBm
	LR		-	-	-	dBm
BLE Modulation Characteristics @ 1Mbps	Δf1 Avg		-	250	-	kHz
	Δf2 Max		-	250	-	kHz
	Δf2 Avg/Δf1 Avg		-	1.38	-	-

Note:

1. There can be up to 2 dB Variation in Tx Power across channels.
2. ETSI Max Power should be limited to 10dBm because, device falls under DTS, non adaptive.
3. In FCC - LR 125kbps Max Power should be limited to 13 dBm to meet PSD requirement because, device falls under DTS, non adaptive.
4. In FCC, Channel 2480MHz ,2Mbps data rate Tx output Power is limited by Band edge.
5. Noise-floor is -159dBm/Hz with spurious tone power is -65dBm at 1601.33 MHz when transmitted signal is at 2402 MHz

7.5.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_BLETX)

Table 7.33. Bluetooth Transmitter Characteristics on 8 dBm RF Chain

Parameter	Condition/Notes	Min	Typ	Max	Units
Transmit Power	LE 1Mbps	-	8	-	dBm
	LE 2Mbps	-	8	-	dBm
	LR 500 Kbps	-	8	-	dBm
	LR 125 kbps	-	8	-	dBm
Adjacent Channel Power |M-N| = 2	LE	-	-32	-	dBm
	LR	-	-	-	dBm
Adjacent Channel Power |M-N| > 2	LE	-	-40	-	dBm
	LR	-	-	-	dBm
BLE Modulation Characteristics @ 1Mbps	Δf1 Avg	-	248	-	kHz
	Δf2 Max	-	249	-	kHz
	Δf2 Avg/Δf1 Avg	-	1.3	-	-

7.5.6 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_RX)

Table 7.34. Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

Parameter	Condition/Notes	Min	Typ	Max	Units
Transmit Power	LE 1Mbps	-	-0.5	-	dBm
	LE 2Mbps	-	-0.5	-	dBm
	LR 500 Kbps	-	-0.5	-	dBm
	LR 125 kbps	-	-0.5	-	dBm
Adjacent Channel Power |M-N| = 2	LE	-	-41	-	dBm
	LR	-	-	-	dBm
Adjacent Channel Power |M-N| > 2	LE	-	-47	-	dBm
	LR	-	-	-	dBm
BLE Modulation Characteristics @ 1Mbps	Δf1 Avg	-	248	-	kHz
	Δf2 Max	-	249	-	kHz
	Δf2 Avg/Δf1 Avg	-	1.3	-	-

7.5.7 Bluetooth Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_RX)

Table 7.35. Bluetooth Receiver Characteristics on HP RF Chain

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1]	LE (1 Mbps), 37 bytes, PER=30.8%	-	-96	-	dBm
	LE (1 Mbps), 255 bytes, PER=30.2%	-	-94	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-93	-	dBm
	LE (2 Mbps), 255 bytes, PER=30.2%	-	-91	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-102.5	-	dBm
	LR (500 Kbps), 255 bytes, PER=30.2%	-	-101.5	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-107	-	dBm
	LR (125 Kbps), 255 bytes, PER=30.2%	-	-106	-	dBm
Maximum Input Level	LE 1Mbps, 2Mbps, 255 bytes PER=30.2%	-	2	-	dBm
	LR 500kps, 125kbps, 255 bytes PER=30.2%	-	3	-	dBm
C/I Performance	LE 1Mbps, co-channel PER=30.8%	-	-10	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	-6	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-4	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	23	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	28	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	29	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	35	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	33	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	25	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	30	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	29	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	-12	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	1	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	-1	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	13	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	19	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	31	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	13	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	26	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	1	-	dB

Note:
1. BLE, LR: Sensitivities for channels 19,39 are up to 2 dB lower performance.

7.5.8 Bluetooth Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_RX)

Table 7.36. Bluetooth Receiver Characteristics on LP RF Chain

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1],[2]	LE (1 Mbps), 37 bytes, PER=30.8%	-	-96	-	dBm
	LE (1 Mbps), 255 bytes, PER=30.2%	-	-94	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-93	-	dBm
	LE (2 Mbps), 255 bytes, PER=30.2%	-	-91	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-102.5	-	dBm
	LR (500 Kbps), 255 bytes, PER=30.2%	-	101.5	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-107	-	dBm
	LR (125 Kbps), 255 bytes, PER=30.2%	-	-106	-	dBm
Maximum Input Level	LE 1Mbps, 2Mbps, 255 bytes, PER=30.2%	-	-4.5	-	dBm
	LR 500kps, 125kbps, 255 bytes, PER=30.2%	-	2.5	-	dBm
C/I Performance	LE 1Mbps, co-channel PER=30.8%	-	-12	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	-6	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-4	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	26	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	28	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	17	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	31	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	33	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	17	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	24	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	17	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	-10	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	-1	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	1	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	13	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	19	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	33	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	13	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	24	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	-1	-	dB

Note:
1. BLE, LR: Sensitivities for channels 19, 39 are up to 2 dB lower performance.

7.6 Typical Current Consumption

1. The below mentioned current numbers will be updated further as SiWx917 validation continues

7.6.1 3.3 V
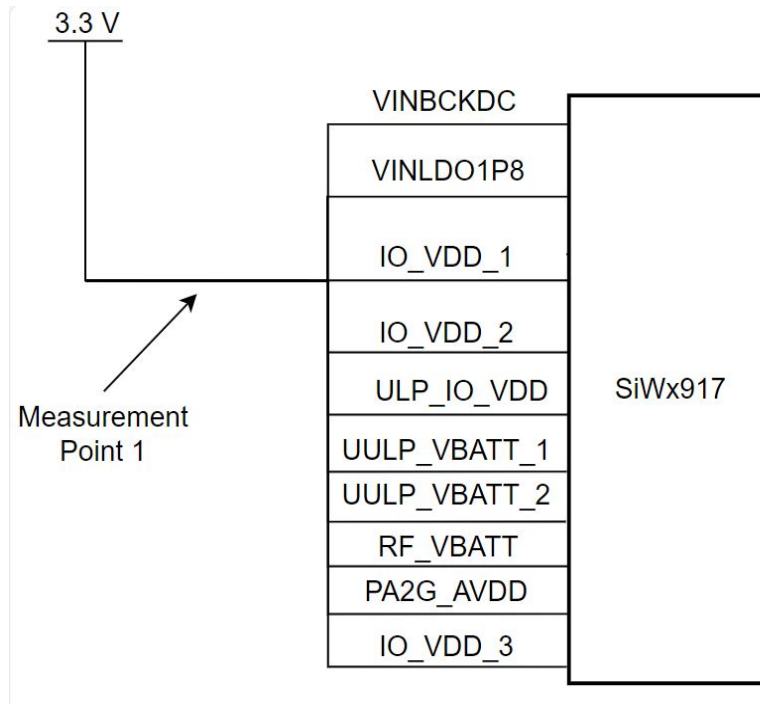
7.6.1.1 WLAN 2.4 GHz

Parameter	Description	Min	Typ	Max	Units
1 Mbps Listen	LP Chain	-	13	-	mA
1 Mbps RX Active	LP Chain	-	18	-	mA
HT20 MCS0 RX	HP Chain	-	51	-	mA
HT20 MCS7 RX	HP Chain	-	51	-	mA
HE20 MCS0 RX	HP chain	-	51	-	mA
HE20 MCS7 RX	HP chain	-	51	-	mA
1 Mbps TX	HP chain	-	260	-	mA
HT20 MCS0 TX	HP Chain	-	230	-	mA
HT20 MCS7 TX	HP Chain	-	180	-	mA
HE20 MCS0 TX	HP Chain	-	212	-	mA
HE20 MCS7 TX	HP Chain	-	173	-	mA
Deep Sleep	No RAM Retained	-	2.5	-	µA
Deep Sleep with RAM Retention	352K RAM Retained	-	9	-	uA
Standby Associated, DTIM = 10 Without TCP Keep alive	WLAN Keep Alive Every 30 secs with 352K RAM Retained	-	55	-	µA
Standby Associated, DTIM = 10 With TCP Keep alive	TCP Keep Alive Every 240 secsWLAN Keep Alive Every 30 secs	-	65	-	µA
11ax TWT With Auto Config Feature Enabled, Without TCP Keep Alive	11ax TWT Rx Latency 2 secs with 8ms Wakeup Duration. WLAN Keep Alive Every 30 secs with 352K RAM Retained	-	80	-	µA
	11ax TWT Rx Latency 30 secs with 8ms Wakeup Duration. WLAN Keep Alive Every 30 secs with 352K RAM Retained	-	32	-	µA
	11ax TWT Rx Latency 60 secs with 8ms Wakeup Duration. WLAN Keep Alive Every 60 secs with 352K RAM Retained	-	20	-	µA
11ax TWT With Auto Config Feature Enabled,With TCP Keep Alive Every 240 secs	11ax TWT Rx Latency 2 secs with 8ms Wakeup Duration. WLAN Keep Alive Every 30 secs with 352K RAM Retained	-	82	-	µA
	11ax TWT Rx Latency 30 secs with 8ms Wakeup Duration. WLAN Keep Alive Every 30 secs with 352K RAM Retained	-	35	-	µA
	11ax TWT Rx Latency 60 secs with 8ms Wakeup Duration. WLAN Keep Alive Every 60 secs with 352K RAM Retained	-	23	-	µA

7.6.1.2 Bluetooth LE

Parameter	Description	Min	Typ	Max	Units
TX Active Current	LP chain, Tx Power = 0 dBm	-	10	-	mA
	LP chain, Tx Power = max transmit power		17		mA
RX Active Current	LP chain	-	10	-	mA
Advertising, Unconnectable	Advertising on all 3 channels with the Advertising payload 37 bytes @ AI = 1.28s , Tx power @0 dBm and LP chain	-	37	-	µA
Advertising, Connectable	Advertising on all 3 channels with the Advertising payload 37 bytes @ AI = 1.28s , Tx power @0 dBm and LP chain	-	41	-	µA
Connected	Connection Interval @1.28s, No data and Tx power @ 0 dBm and LP chain	-	36	-	µA
Connected	Connection Interval @200msec, No data and Tx power @ 0 dBm and LP chain	-	115	-	µA

8. Reference Schematics, BOM and Layout Guidelines

8.1 SiWN917 QFN

8.1.1 Schematics

The below diagram shows the typical schematic for NCP mode. Please refer to following documents for more information.

- Follow Crystal calibration Application note for calibrating the external 40MHz crystal.
- Follow Gain offset calibration Application note for calibrating the power of RF front-end circuitry.
- Follow RF Matching and Layout Design Guide Application note for RF design related aspects.
   1. Customers should include provision for programming or updating the firmware at manufacturing.
   2. If using UART, we recommend bringing out the SPI lines to test points, so designers could use the faster interface for programming the firmware as needed.
   3. If using SPI as host interface, then firmware programming or update can be done through the host MCU, or if designer prefers to program standalone at manufacturing, then it is recommended to have test points on the SPI signals.
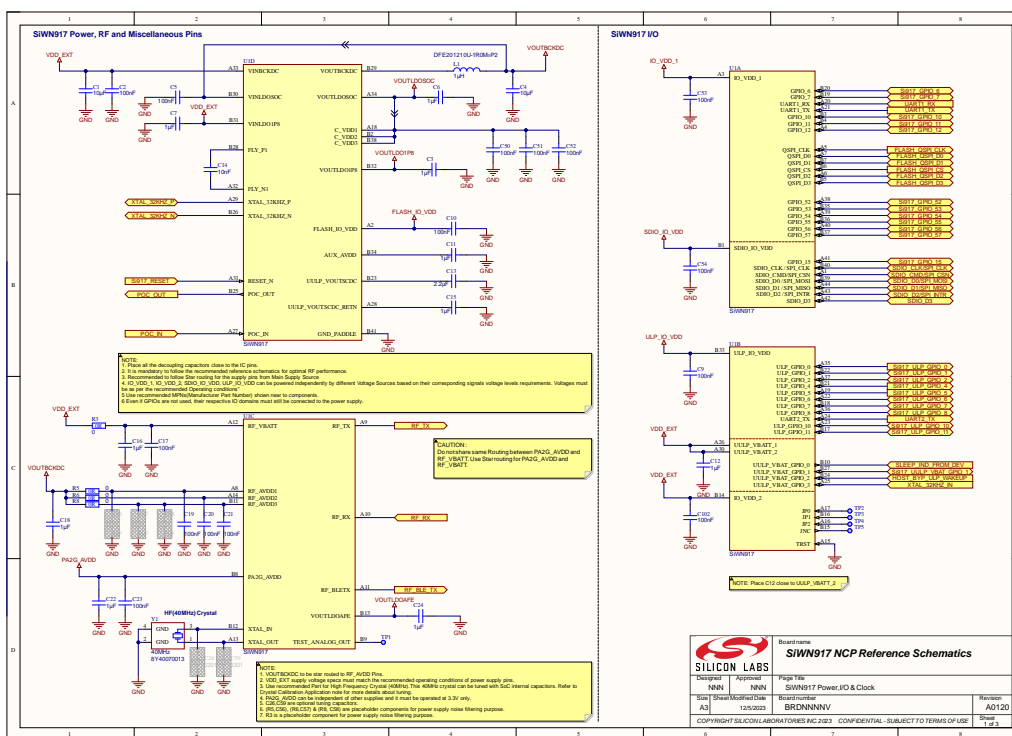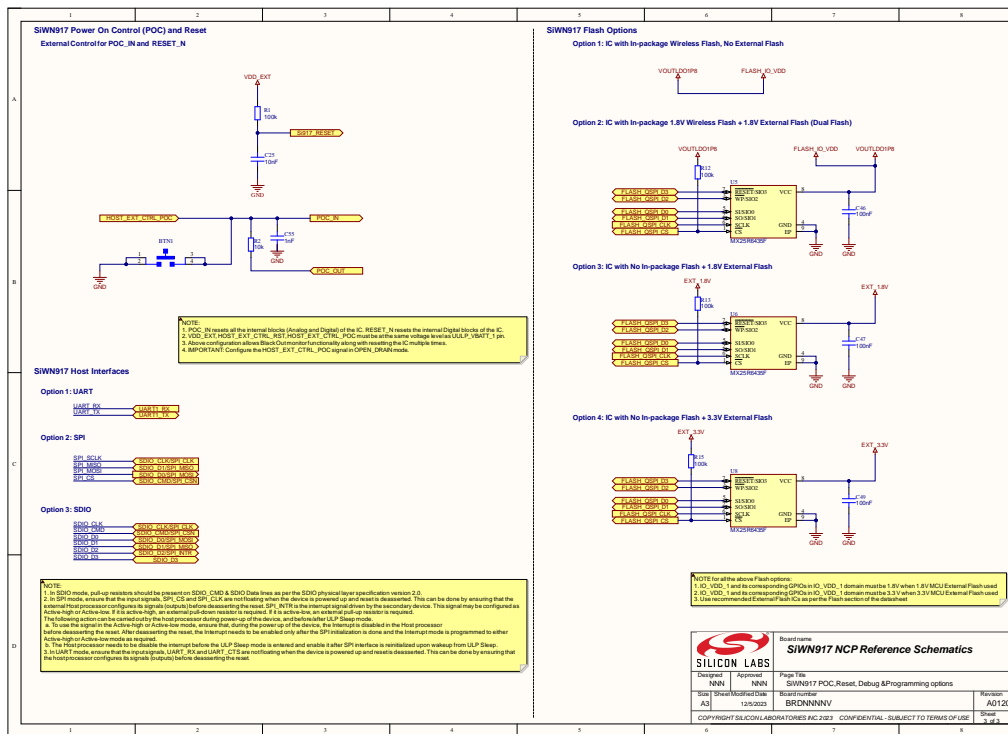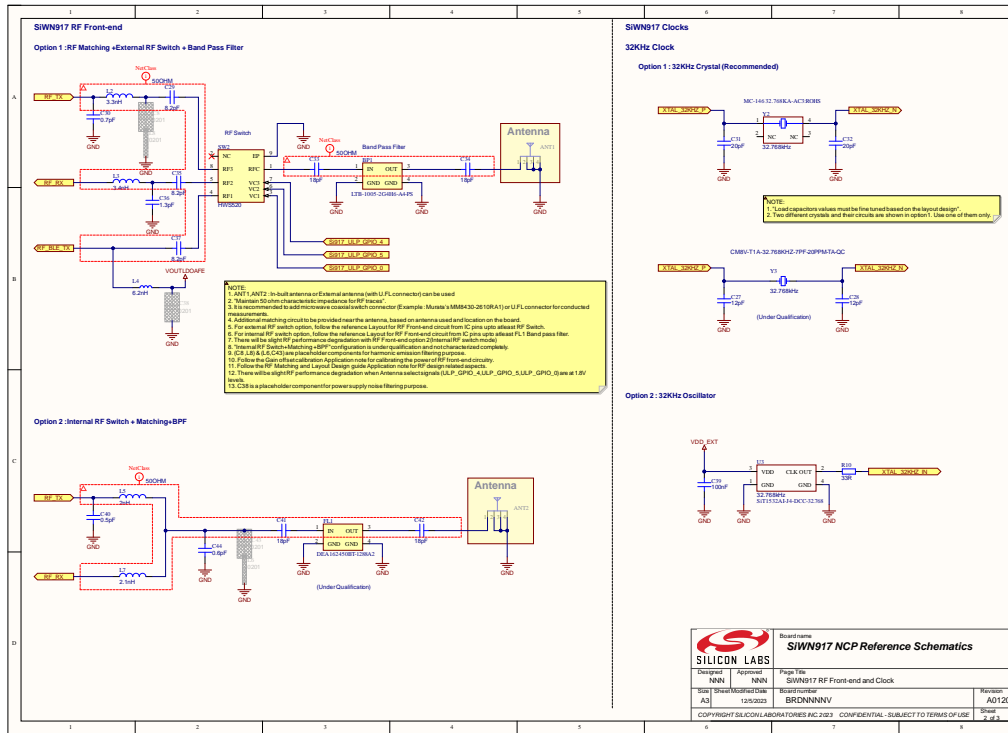
Figure 8.1. QFN NCP Schematics

8.1.2 BOM

Table 8.1. SiWN917 Circuitry: Mandatory Components (Power Mangement + Crystal + SiWN917 IC)

S.No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
1	1	C1	10µF	Murata	GRM188R61C106MAALD	CAP CER 0603 X5R 10uF 16V 20%
2	10	C2, C5, C9, C10, C50, C51, C52, C53, C54, C102	100nF	Murata	GRT155R71H104KE01D	CAP CER 0402 X7R 0.1uF 50V 10%
3	10	C3, C6, C7, C11, C12, C15, C16, C18, C22, C24	1µF	Murata	GRM033R61C105ME15D	CAP CER 0201 X5R 1uF 16V 20%
4	1	C4	10µF	CalChip	GMC21X7R106K25NT	CAP CER 0805 X7R 10uF 25V 10%
5	1	C13	2.2µF	Murata	GRM033R61A225ME47D	CAP CER 0201 X5R 2.2uF 10V 20%
6	1	C14	10nF	Murata	GRM033R61C103KA12D	CAP CER 0201 X5R 10nF 16V 10%
7	5	C17, C19, C20, C21, C23	100nF	Murata	GRM033R61C104KE14J	CAP CER 0201 X5R 100nF 16V 10%
8	1	L1	1µH	Murata	DFE201210U-1R0M=P2	IND Fixed 0805 1uH 2A 95mOhm 20%
9	4	R3, R5, R6, R8	0	Yageo	RC0201FR-07200RL	RES 0201 0R
10	1	U1	SiWN917	Silicon Labs	SiWN917	Choose the suitable OPN from List of OPNs from Ordering In-formation section in datasheet.
11	1	Y1	40MHz	TXC	8Y40070013	CRYSTAL 2.0X1.6mm 40MHz 8pF 8ppm

Table 8.2. SiWN917: RF Front-End Options (one of them has to be used mandatorily)

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
Option 1: RF Matching +External RF Switch + Band Pass Filter						
12	1	ANT1	2.4GHz	Johanson	2450AT18D0100001	ANT SMD 3.2X1.6X1.2MM 2.4GHz
13	1	BP1	2.45GHz	Maglayers	LTB-1005-2G4H6-A4-PS	FILTER BAND PASS 0402-4Pin 2.45GHz 100MHz
14	3	C29, C35, C37	8.2pF	Murata	GJM0335C1E8R2BB01	CAP CER 0201 C0G 8.2pF 25V ±0.1pF
15	1	C30	0.7pF	Murata	GJM0335C1HR70WB01	CAP CER 0201 C0G 0.7pF 50V ±0.05pF

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
16	2	C33, C34	18pF	Murata	GRM0335C1H180GA01	CAP CER 0201 C0G 18pF 50V 2%
17	1	C36	1.3pF	Murata	GRM0335C1E1R3WA01D	CAP CER 0201 C0G 1.3pF 25V ±0.05pF
18	1	L2	3.3nH	Murata	LQP03TQ3N3B02	IND Fixed 0201 3.3nH 450mA 240mOhm ±0.1nH
19	1	L3	3.4nH	Murata	LQP03TQ3N4C02	IND Fixed 0201 3.4nH 450mA 250mOhm ±0.2nH
20	1	L4	6.2nH	Murata	LQP03HQ6N2H02	IND Fixed 0201 6.2nH 400mA 250mOhm 3%
21	1	SW2	HWS520	Hexawave	HWS520	IC RF SWITCH SP3T 6GHz USON8L
Option 2: Internal RF Switch + Matching + BPF						
22	1	ANT2	2.4GHz	Johanson	2450AT18D0100001	ANT SMD 3.2X1.6X1.2MM 2.4GHz
23	2	C41, C42	18pF	Murata	GRM0335C1H180GA01	CAP CER 0201 C0G 18pF 50V 2%
24	1	C40	0.5pF	Murata	GRM0335C1HR50WA01	CAP CER 0201 C0G 0.5pF 50V ±0.05pF
25	1	C44	0.6pF	Murata	GJM0335C1ER60WB01	CAP CER 0201 C0G 0.60pF 25V ±0.05pF
26	1	FL1	2.45GHz	TDK	DEA162450BT-1288A2	FILTER BAND PASS 1608 2400MHz 2500MHz
27	1	L5	2nH	Murata	LQP03TN2N0B02D	IND Fixed 0201 2nH 600mA 150mOhm ±0.1nH
28	1	L7	2.1nH	Murata	LQP03TN2N1B02	IND Fixed 0201 2.1nH 600mA 150mOhm ±0.1nH

Table 8.3. SiWN917: External 32KHz Clock Options (these are optional and need not be used for every use-case)

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
Option 1a: 32KHz Crystal (Qualified)						
29	1	Y2	32.768kHz	Epson	MC-146 32.768KA-AC3:ROHS	CRYSTAL 7.0x1.5mm 32.768kHz 9pF 20ppm
30	2	C31, C32	20pF	Murata	GRM0335C1H200GA01	CAP CER 0201 C0G 20pF 50V 2%
Option 1b: 32KHz Crystal (Under Qualification)						
31	2	C27, C28	9pF	Murata	GJM0335C1E9R0WB01	CAP CER 0201 C0G 9pF 25V ±0.05pF
32	1	Y3	32.768kHz	Micro Crystal	CM8V-T1A-32.768KHZ-7PF-20PPM-TA-QC	CRYSTAL 2.0x1.2mm 32.768kHz 7pF 20ppm
Option 2: 32KHz Oscillator						

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
33	1	C39	100nF	Murata	GRM033R61C104KE14J	CAP CER 0201 X5R 100nF 16V 10%
34	1	R10	33R	Yageo	RC0201FR-0733RL	RES 0201 33R 1/20W 1% 200ppm
35	1	U3	32.768kHz	SiTIME	SiT1532AI-J4-DCC-32.768	CRYSTAL CSPBGA 32.768kHz 10pF 100ppm

Table 8.4. SiWN917 : External Flash options (these are optional, and need not be used for every use-case)

S. No.	Quanti- ty	Designator	Value	Manufacturer	Manufacturer PN	Description
36	3	C46, C47, C49	100nF	Murata	GRM033R61C104KE14J	CAP CER 0201 X5R 100nF 16V 10%
37	3	R12, R13, R15	100k	Yageo	RC0201FR-07100KL	RES 0201 100K 1/20W 1% 200ppm
39	3	U5, U6, U8	MX25R6435F	Macronix	MX25R6435FM2IL0	IC FLASH 64MBIT SPI/QUAD 8SOP

Table 8.5. SiWN917: Discrete Parts (these are optional: RC circuits with Buttons for RESET_N & POC_IN pins). These need not be used for every use-case)

S. No.	Quanti- ty	Designator	Value	Manufacturer	Manufacturer PN	Description
40	1	BTN1	PTS810 SJM 250 SMTR LFS	C&K	PTS810 SJM 250 SMTR LFS	Tactile Switch SPST-NO 0.05A 16V
41	1	R1	100k	Yageo	RC0201FR-07100KL	RES 0201 100K 1/20W 1% 200ppm
42	1	C25	10nF	Murata	GRM033R61C103KA12D	CAP CER 0201 X5R 10nF 16V 10%
43	1	R2	10k	Yageo	RC0201FR-0710KL	RES 0201 10K 1/20W 1% 200ppm
44	1	C25	1nF	Murata	GRM033R71C102KA01D	CAP CER 0201 X7R 1nF 16V 10%

8.2 Layout Guidelines for QFN

The following guidelines outline the integration of the QFN:

1. The following Supply Pins needs to be Star routed from the Supply Source
   a. VINBCKDC
   b. VINLDO1P8
   c. IO_VDD_1, IO_VDD_2, IO_VDD_3
   d. ULP_IO_VDD
   e. UULP_VBATT_1
   f. UULP_VBATT_2
   g. RF_VBATT
   h. PA2G_AVDD
2. The RF_PORT signal may be directly connected to an on-board chip antenna or terminated in an RF connector of any form factor for enabling the use of external antennas.
3. There need to be DC blocking capacitors (8.2pF) on RF_PORT if connected to Antenna
4. The RF trace on RF_OUT should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
5. To evaluate transmit and receive performance like Tx Power and EVM, Rx sensitivity and the like, an RF connector would be required. A suggestion is to place a 'microwave coaxial connector with switch' between RF_OUT and the antenna.

6. The layout guidelines for BUCK are as follows:

Minimize the loop area formed by inductor switching node, output capacitors & input capacitors. This helps keep high current paths as short as possible. Keeping high current paths shorter and wider would help decrease trace inductance & resistance. This would significantly help increase the efficiency in high current applications. This reduced loop area would also help in reducing the radiated EMI that may affect nearby components .

a. VINBCKDC Capacitor should be very close to the Module Pin & the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.

b. Buck Inductor should be close to Module VOUTBCKDC pin and buck capacitor should be placed closed to the Inductor, the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.

c. The Ground Plane underneath the Buck Inductor in the Top Layer should be made as an isolated copper patch and should descend down to the Second Layer (Main Ground) through multiple Vias.

d. The path from VOUTBCKDC to VINLDOSOC is a high current path. The Trace should be as short & wide as possible and is recommended to run a Grounded Shield Traces on either side of this High Current Trace

e. The Capacitor on VINLDOSOC should be very close to the Module Pin & the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
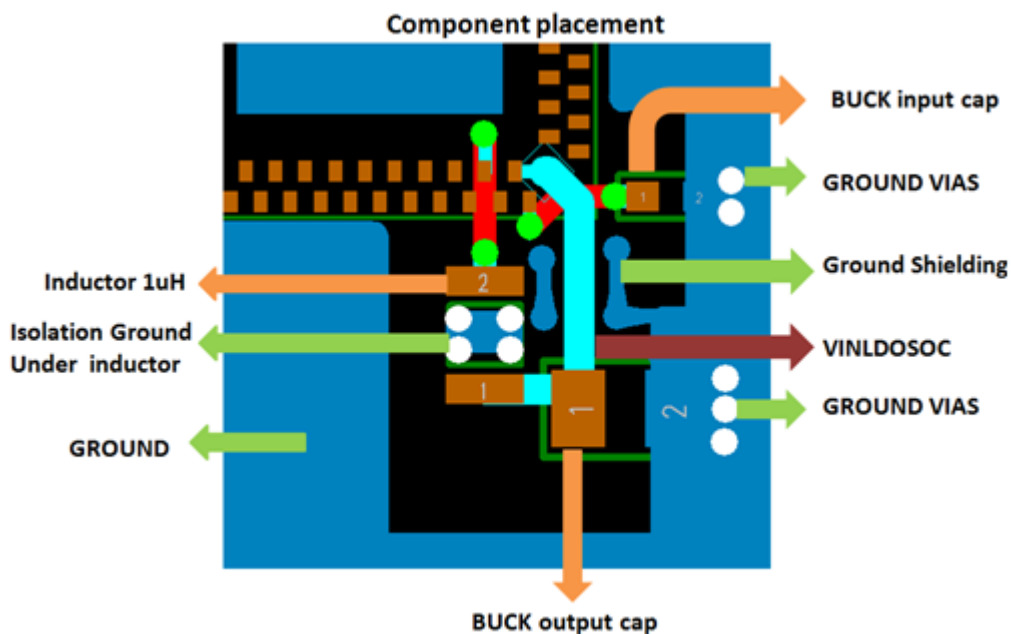
Figure 8.2. BUCK Layout Guidelines

7. Each GND pin must have a separate GND via.

8. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.

9. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.

10. Add GND copper pour underneath IC/Module in all layers, for better thermal dissipation.

11. Provision an RF shield around the IC and RF circuitry, excluding antenna portion.

12. Refer to RF Matching and Layout Design Guide Application Note for more details about following RF related design aspects

13. Add 5 x 5 thermal vias (25 total) of at least 10-mils drill size equally placed on the "GND paddle" for better thermal dissipation.

8.3 Calibration Requirements

The IC design circuit, as shown in Section , involves discrete components in the RF path and 50-ohm PCB traces. There can be variations in manufacturing tolerances from these discrete components and part-to-part IC variation leading to board-to-board performance variation in power level.

Accurate control over TX power is required for regulatory purposes. It is recommended that one performs Tx Gain offset calibration on the end-product to compensate for these board-to-board power variations. This requires provision for conducted power measurement on end-product. If the customer does not have the capability for conducted power measurement and this calibration, then fixed Tx power back off may be required to ensure regulatory compliance.

Refer to application notes that describe the procedure for IC customers to implement at end-product manufacturing flow. These documents explain the procedure for the following:

• Calibration of carrier frequency offset
• Calibration for Tx gain offset on end-product

9. Package Specifications

9.1 Package Outline

Table 9.1. Package Dimensions - QFN

Parameter	Value (LxWxH)	Units
Package Dimensions	7 x 7 x 0.85	mm
Tolerance	±0.1	mm
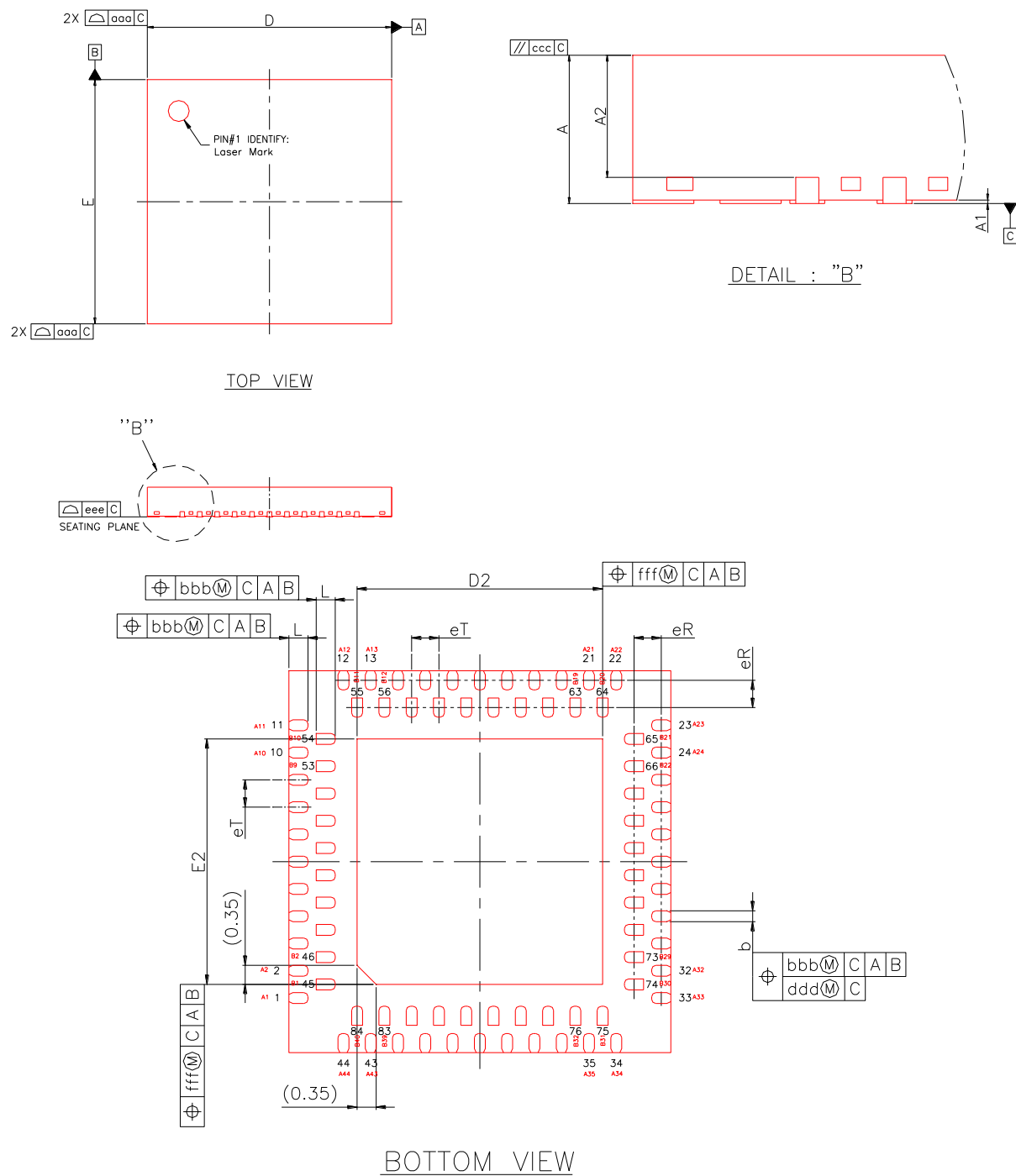
Figure 9.1. Package Outline - QFN

Table 9.2. PCB Landing Pattern - QFN

Dimension	MIN	NOM	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.65	0.70	0.75
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
eT	0.50 BSC		
eR	0.50 BSC		
L	0.30	0.35	0.40
aaa	0.10		
bbb	0.10		
ccc	0.20		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 PCB Land Pattern
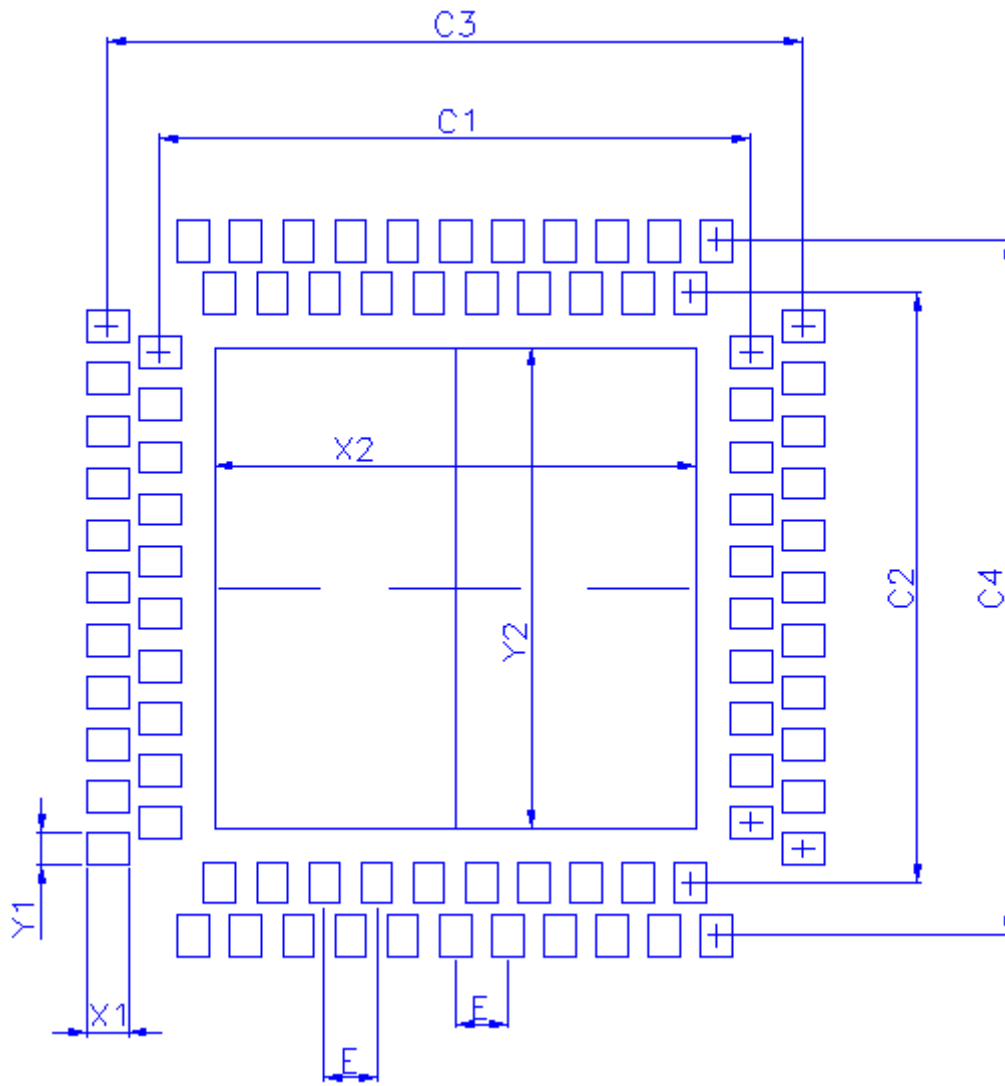
Figure 9.2. PCB Landing Pattern - QFN

Table 9.3. Dimension Table

Dimension	mm
C1	5.55
C2	5.55
C3	6.55
C4	6.55
E	0.5 BSC
X1	0.4
X2	4.60
Y1	0.25
Y2	4.60

Dimension	mm

Note:
 	
General
 	
  1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05mm is assumed.
 	
  2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
 	
Solder Mask Design
 	
  1. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 0.1mm minimum, all the way around the pad.
 	
Stencil Design
 	
  1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
 	
  2. The stencil thickness should be 0.100mm (4 mils).
 	
  3. The stencil aperture to land pad size recommendation is 80% paste coverage.
 	
*Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.	

9.3 Top Marking
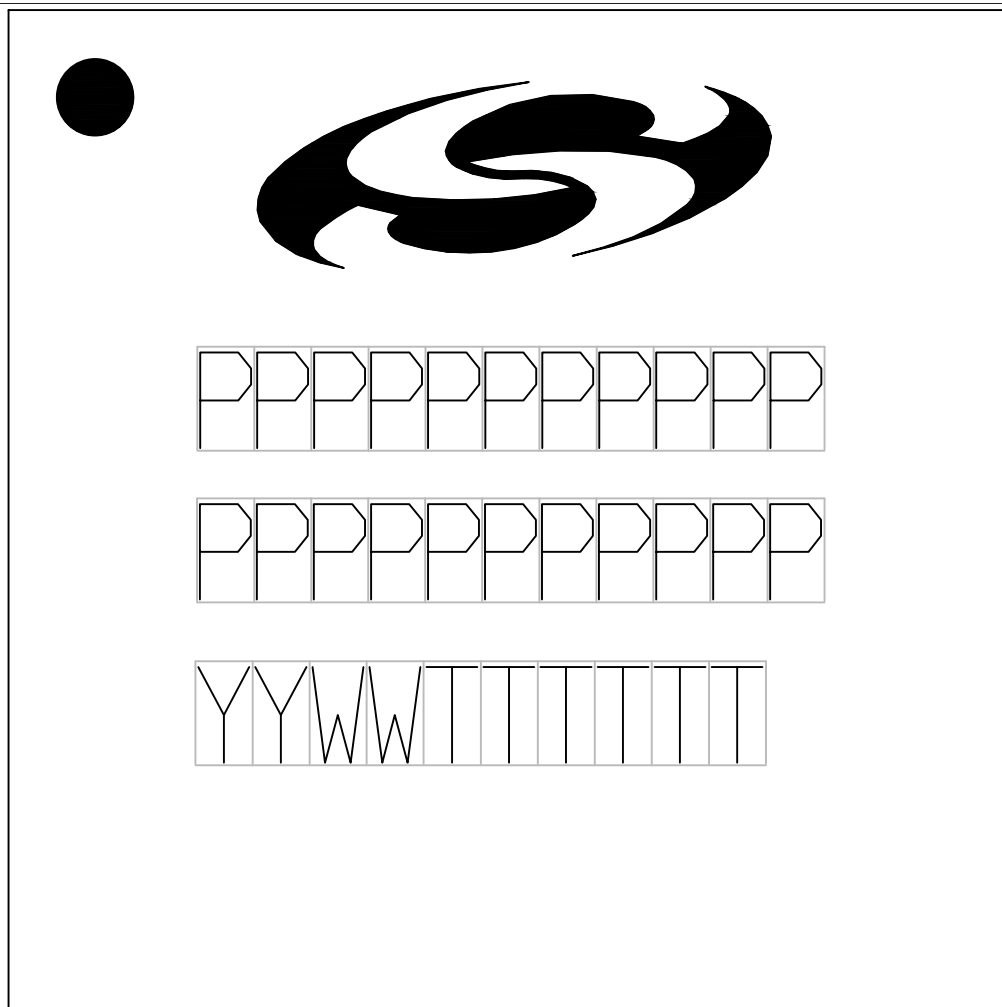
Figure 9.3. Top Marking

Mark Description

The package marking consists of:

- PPPPPPPPPPP - Part number designation in both the rows
- YYWWTTTTTT
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - TTTTTT – A trace or manufacturing code. The first letter is the device revison.

10. SiWx917 Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using SiWx917. These documents will be available on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

Resource Location

SiWx917 Document Library: https://docs.silabs.com/wiseconnect/3.1.0/wiseconnect-developing-with-wiseconnect-sdk/

Technical Support: http://www.silabs.com/support/

11. Revision History

Revision 0.5

December, 2023

Updated Section 2. Ordering Information

Updated Table 6.3 Chip Packages - Peripheral Interfaces on page 18

Updated Table 7.5 DCDC Switching Converter Electrical Specifications on page 31

Updated Table 7.6 SoC LDO Electrical Specifications on page 31

Updated Section 7.6.1.1 WLAN 2.4 GHz

Revision 0.1

October, 2023

Initial draft.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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